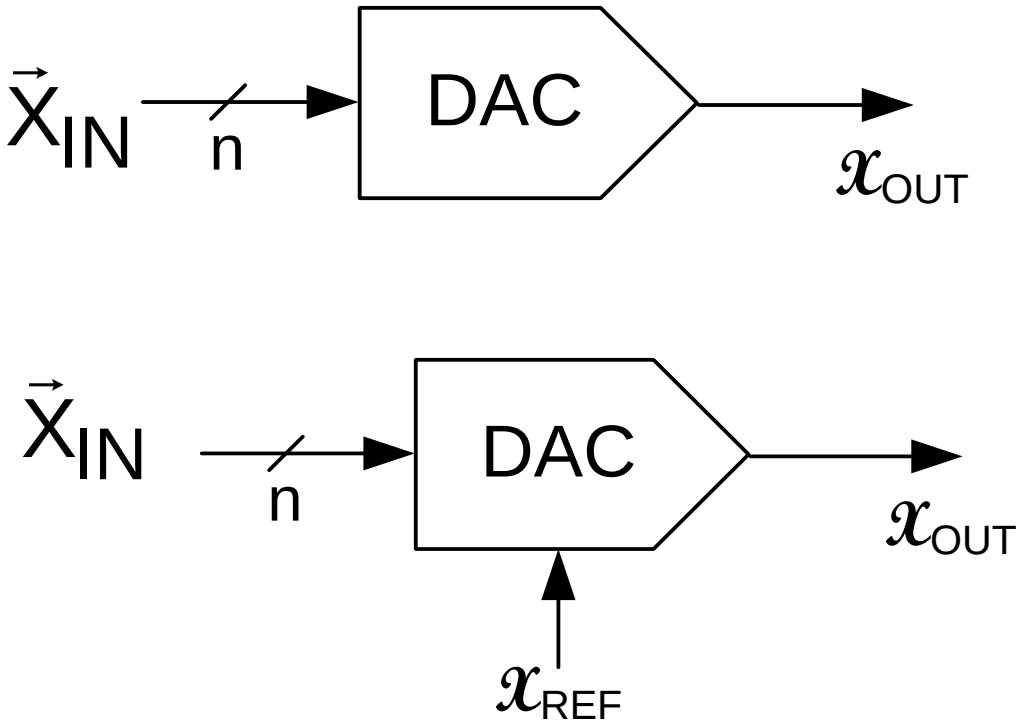
EE 505

Lecture 2
Data Converter Operation and Characterization

REVIEW from LAST LECTURE

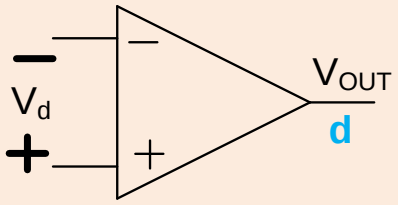
D/A Converters

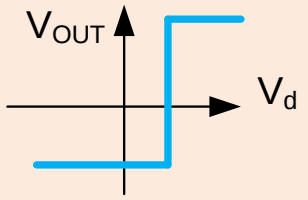


REVIEW from LAST LECTURE

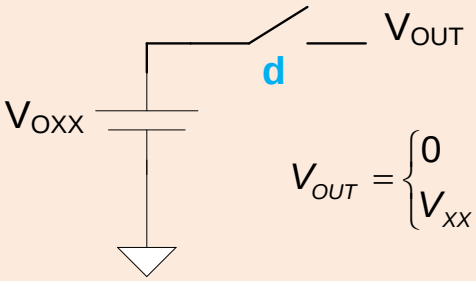
Data Converters

Electronic Data Conversion Process:





ADC



DAC

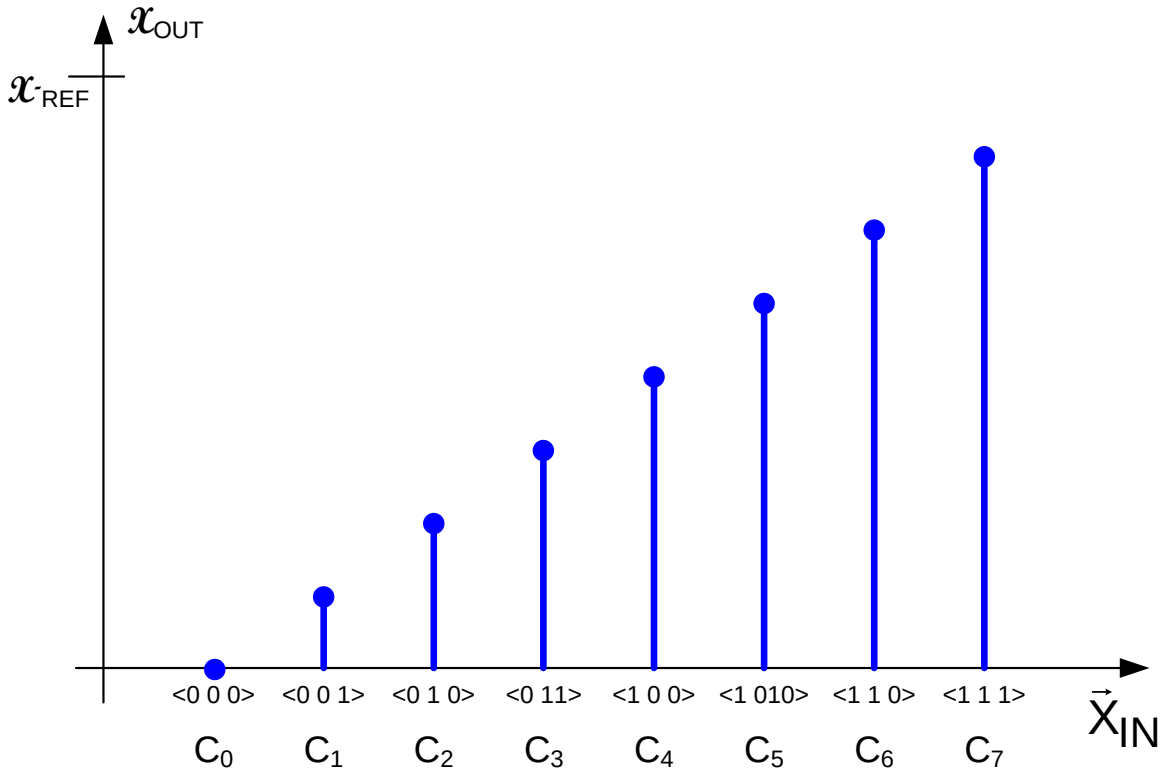
- The comparator is the basic analog to digital conversion element in all ADCs
- The switch is the basic digital to analog conversion element in all DACs
- Data converters incorporate one or more basic ADC or DAC cells
- Design of comparator or switch is often critical in data converters
- Performance of data converters often dependent upon performance of comparator, switch, and matching

REVIEW from LAST LECTURE

D/A Converters

$\vec{X}_{IN}=<b_{n-1},b_{n-1},...b_1,b_0>$

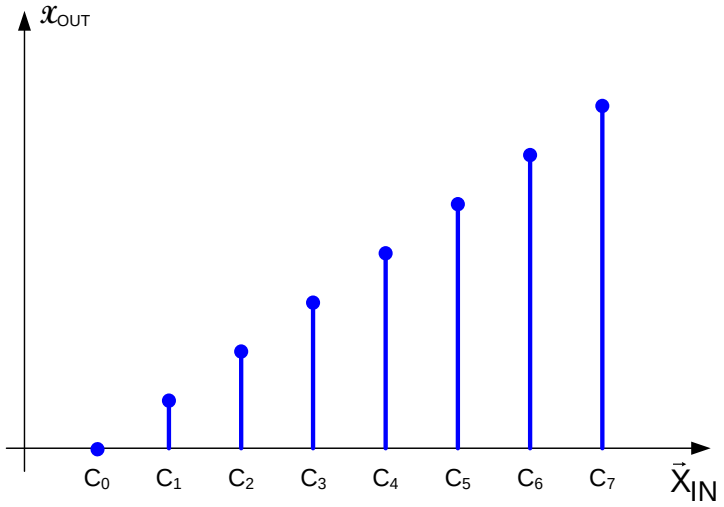
An Ideal DAC transfer characteristic (3-bits)



Code C_k is used to represent the decimal equivalent of the binary number $<b_{n-1} .. b_0)>$

REVIEW from LAST LECTURE

D/A Converters



For this ideal DAC

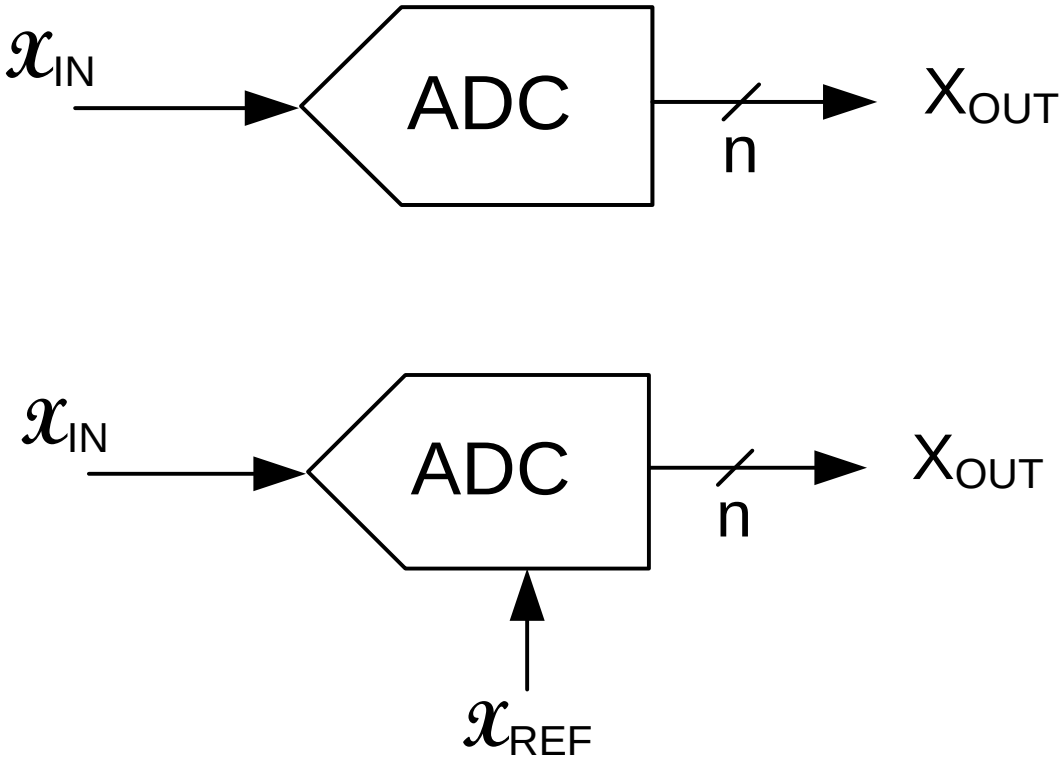
$$X_{OUT}=X_{REF}\left(\frac{b_{n-1}}{2}+\frac{b_{n-2}}{4}+\frac{b_{n-3}}{8}+\ldots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)$$

$$X_{OUT}=X_{REF}\sum_{j=1}^{n}\frac{b_{n-j}}{2^j}$$

- Number of outputs gets very large for n large
- Spacing between outputs is $X_{REF}/2^n$ and gets very small for n large

REVIEW from LAST LECTURE

A/D Converters



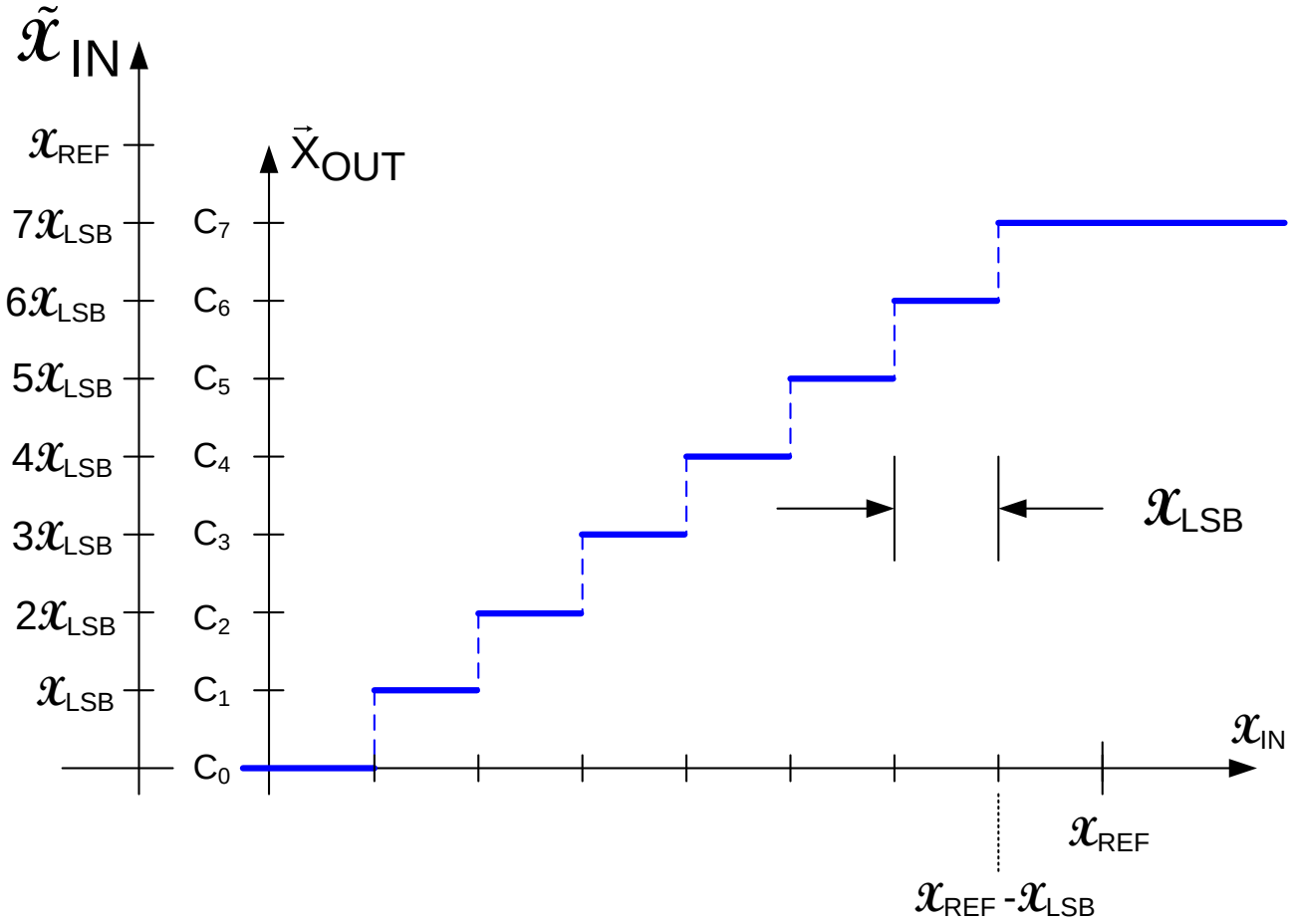
REVIEW from LAST LECTURE

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$

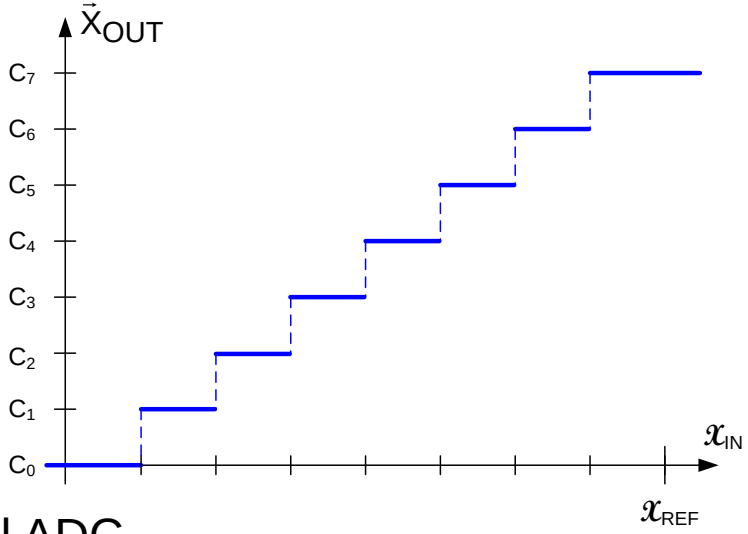
$$x_{LSB} = \frac{x_{REF}}{2^n}$$



The second vertical axis, labeled $\tilde{x}_{IN}$ is the interpreted value of x_{IN}

REVIEW from LAST LECTURE

A/D Converters



For this ideal ADC

$$\tilde{x}_{OUT} = x_{REF}\left(\frac{d_{n-1}}{2}+\frac{d_{n-2}}{4}+\frac{d_{n-3}}{8}+\ldots+\frac{d_1}{2^{n-1}}+\frac{d_0}{2^n}\right)$$

$$\tilde{x}_{OUT} - x_{IN} = \varepsilon$$

where ε is small (typically less than 1LSB)

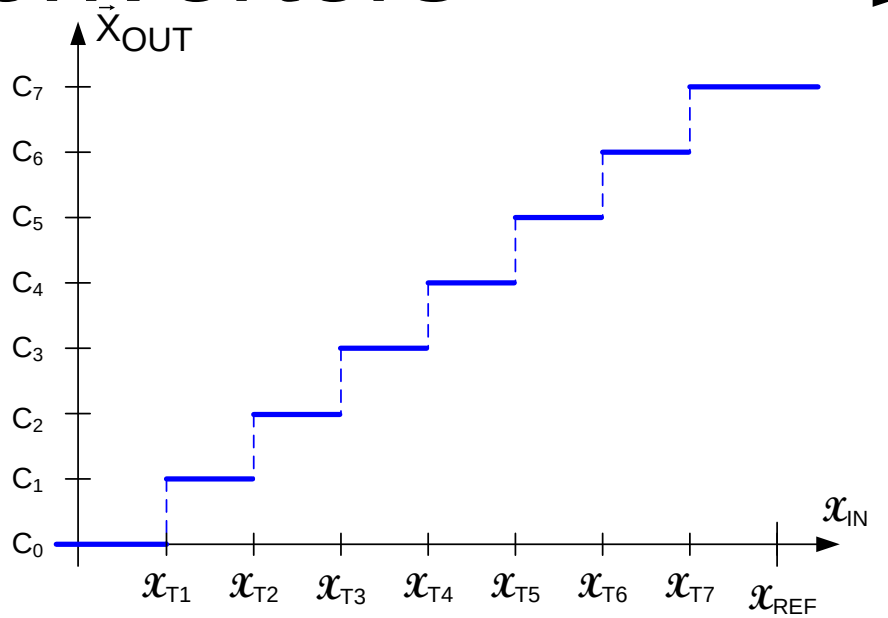
$$x_{IN} = x_{REF}\sum_{j=1}^{n}\frac{d_{n-j}}{2^j} - \varepsilon$$

- Number of bins gets very large for n large
- Spacing between break points is $x_{REF}/2^n$ and gets very small for n large

ε is the **quantization error** and is inherent in any ADC

REVIEW from LAST LECTURE

A/D Converters



Transition Points

- Actual values of x_{IN} where transitions occur are termed transition points or break points
- For an ideal n-bit ADC, there are 2^n-1 transition points
- Ideally the transition points are all separated by 1 LSB -- $X_{LSB}=X_{REF}/2^n$
- Ideally the transition points are uniformly spaced
- In an actual ADC, the transition points will deviate a little from their ideal location

Labeling Convention:

We will define the transition point X_{Tk} to be the break point where the transition in the code output to code C_k occurs. This seemingly obvious ordering of break points becomes ambiguous, though, when more than one break points cause a transition to code C_k which can occur in some nonideal ADCs

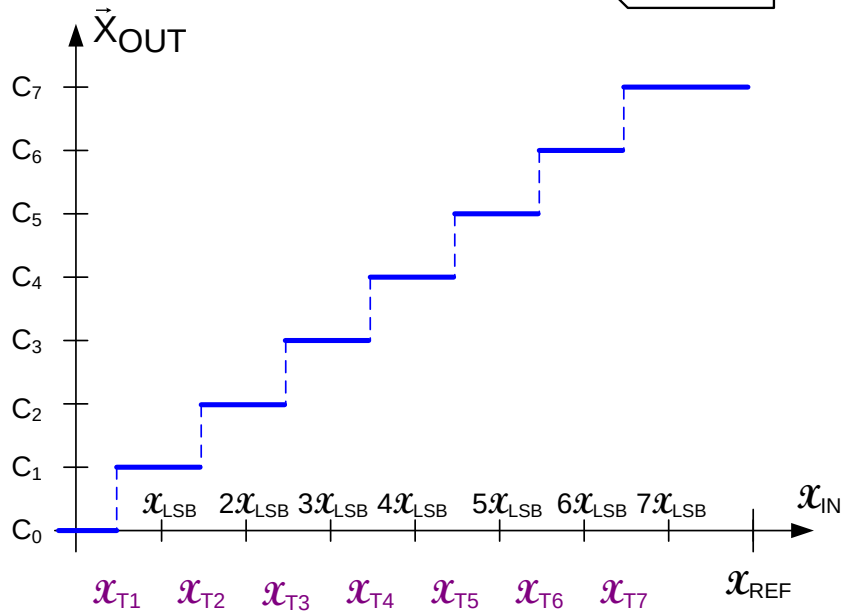
REVIEW from LAST LECTURE

A/D Converters

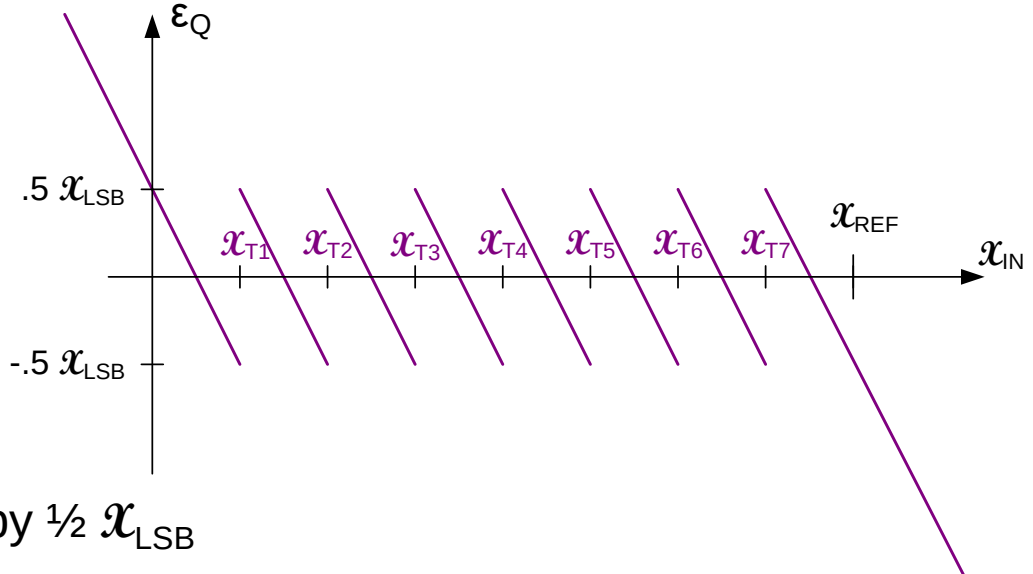
Quantization Errors

Another Ideal ADC

$x_{T1}=x_{LSB}/2$



$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$



Magnitude of ε_Q bounded by ½ x_{LSB}

REVIEW from LAST LECTURE

Characterization of Data Converter Performance

- Almost all ADC architectures will work perfectly if nonideal effects are ignored !!
- Most data converter design effort involves managing nonideal properties of components
- “Devil is often in the detail” when designing an ADC

Critical to know how to accurately characterize an ADC

What may appear to be minor differences in performance are often differentiators in both the marketplace and in the profit potential of a part

REVIEW from LAST LECTURE

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Performance Characterization of Data Converters

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

REVIEW from LAST LECTURE

Dynamic characteristics

- Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance

- Dynamic characteristics often high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the 6n+6 bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better. If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{(-90dB/20dB)} = 32\mu V$ level. A 32uV level is about 1part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.

Performance Characterization of Data Converters

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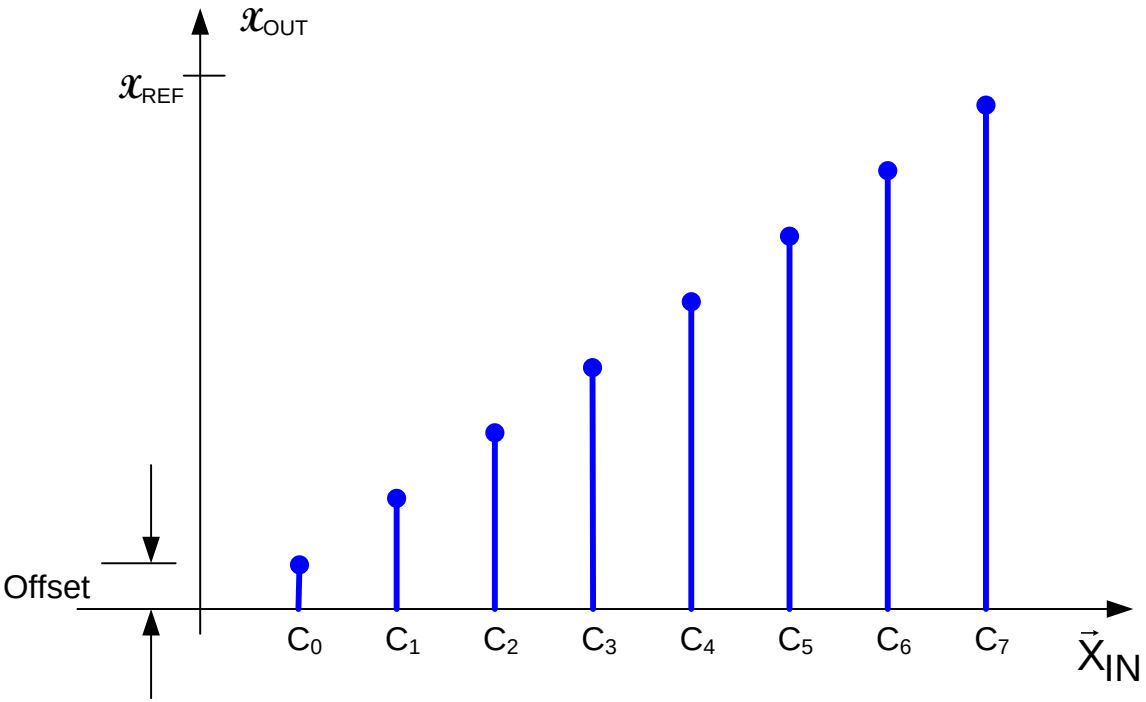
Performance Characterization

Offset

For DAC with ideal code 0 output of 0V the offset is

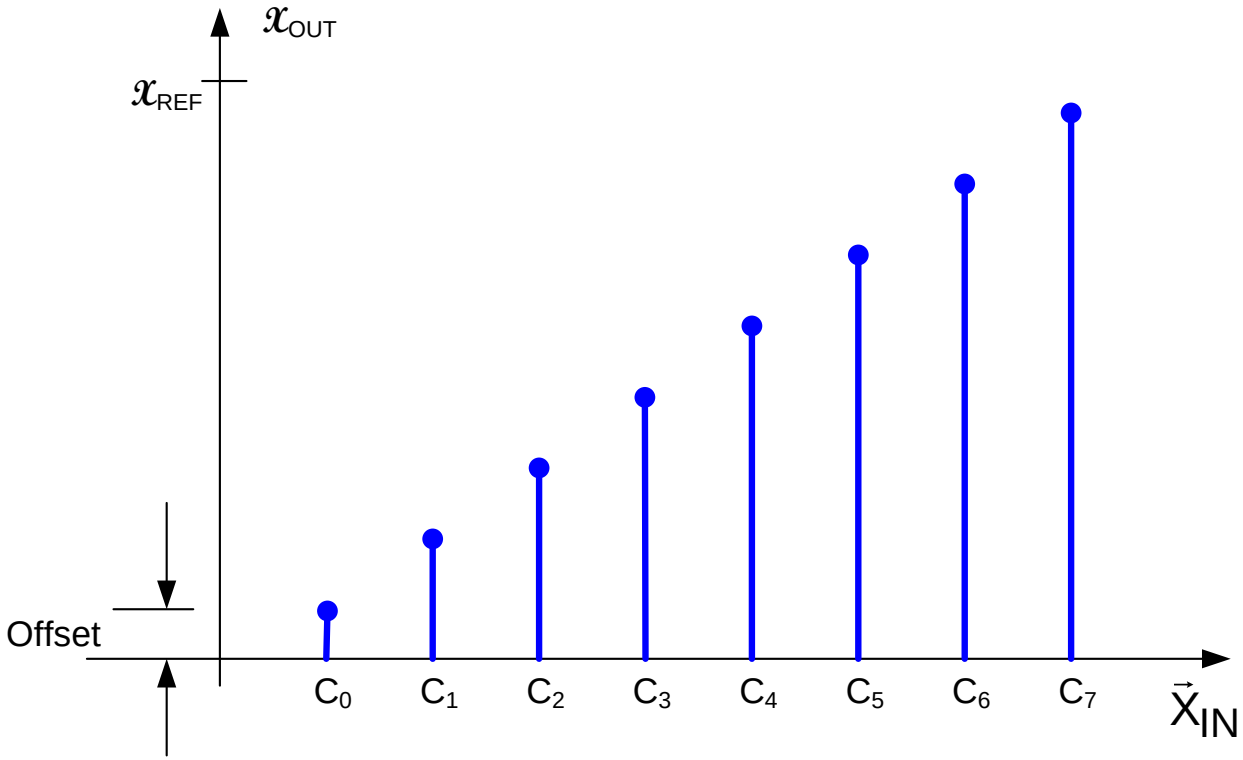
$x_{OUT}(<0,\ldots,0>)$ - absolute

$\frac{x_{OUT}(\langle 0,\ldots,0\rangle)}{x_{LSB}}$ - in LSB



Performance Characterization

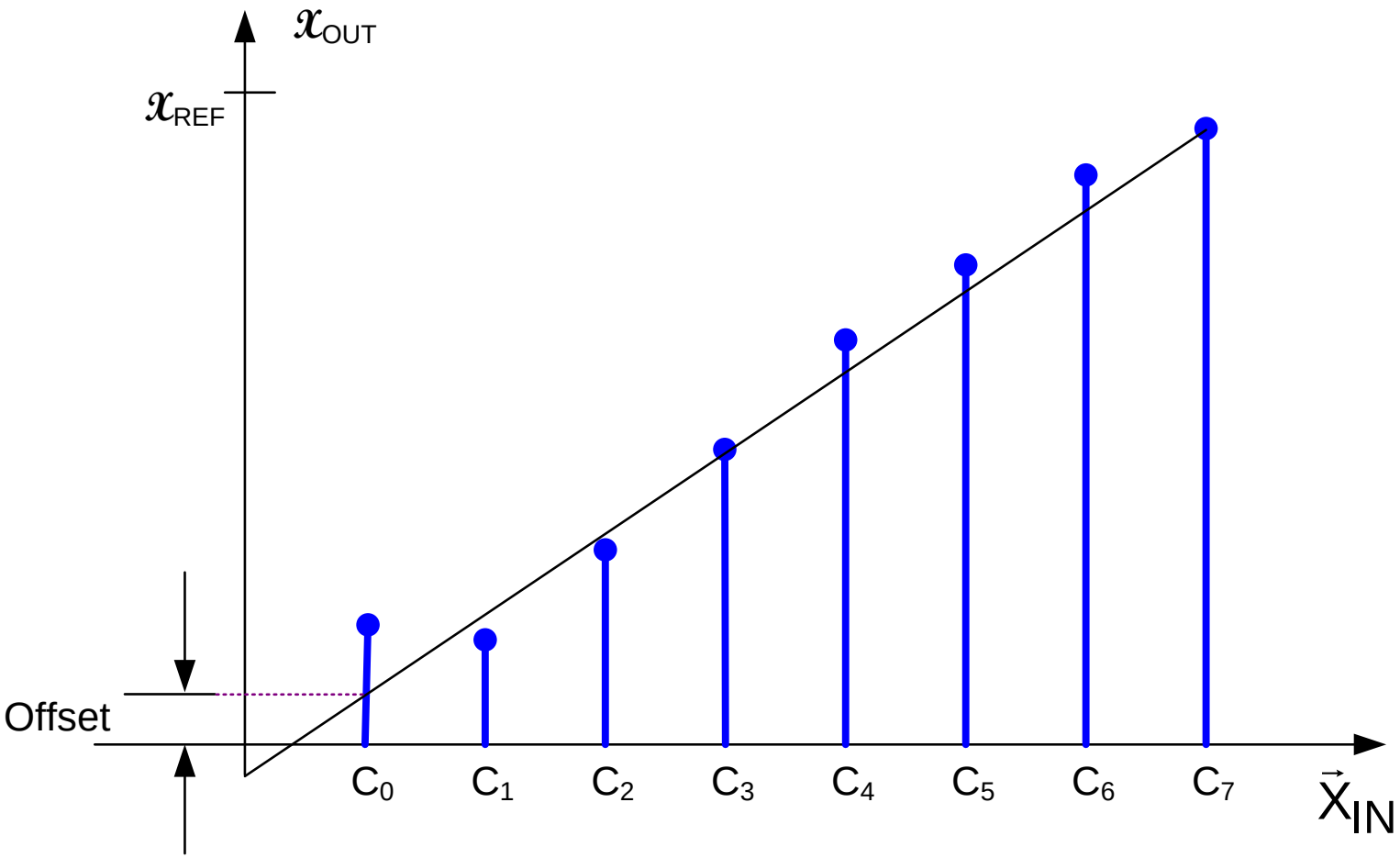
Offset (for DAC)



- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data

Performance Characterization

Offset (for DAC)



Offset relative to fit of data

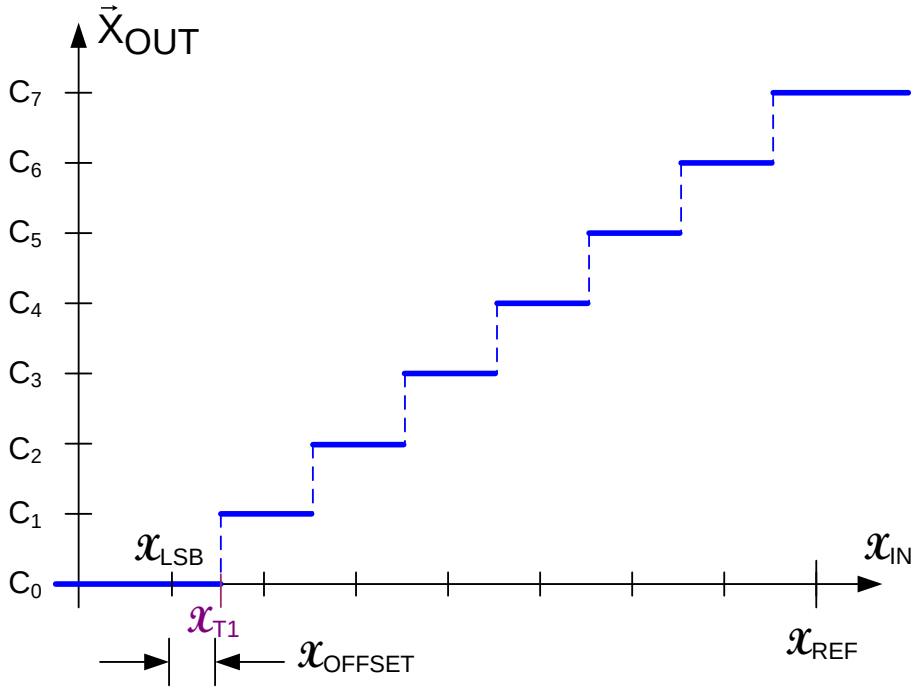
Performance Characterization

Offset

For ADC with ideal transition point at 1 LSB, the offset is

$x_{T1} - x_{LSB}$ - absolute

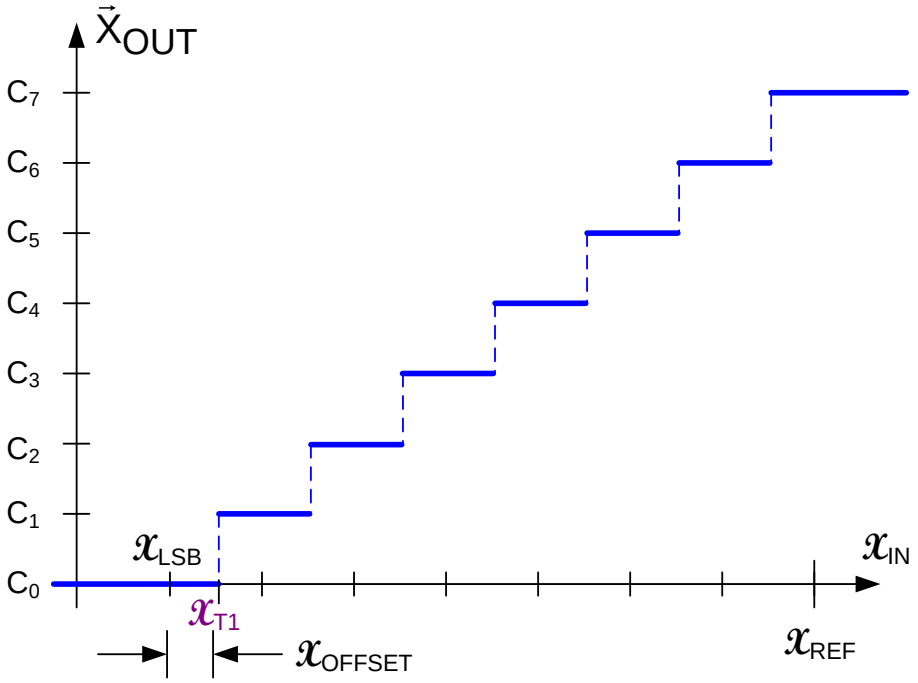
$\frac{x_{T1} - x_{LSB}}{x_{LSB}}$ - in LSB



Performance Characterization

Offset

For ADC the offset is



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Performance Characterization

Offset

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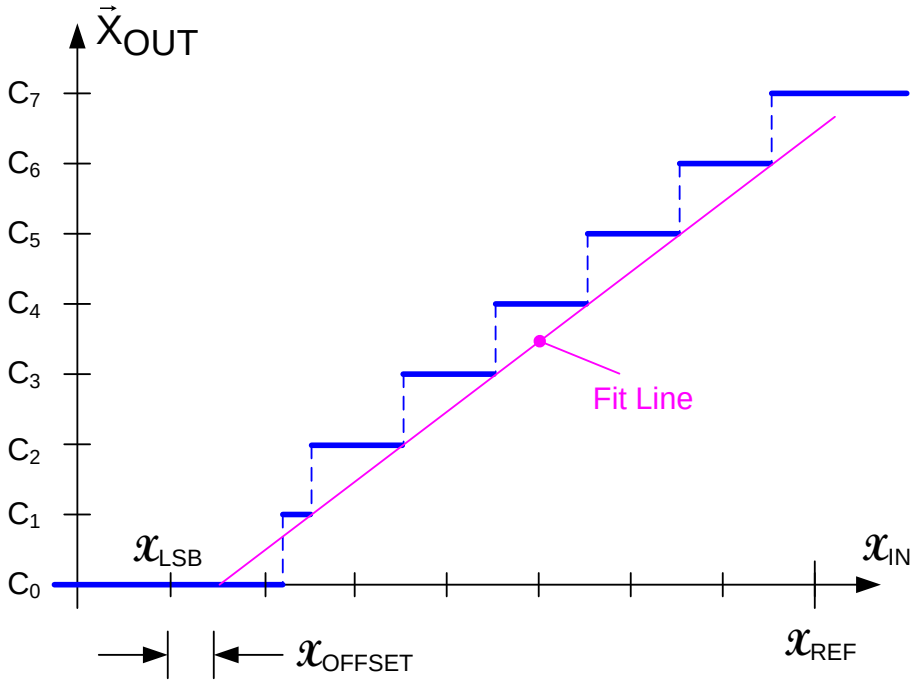
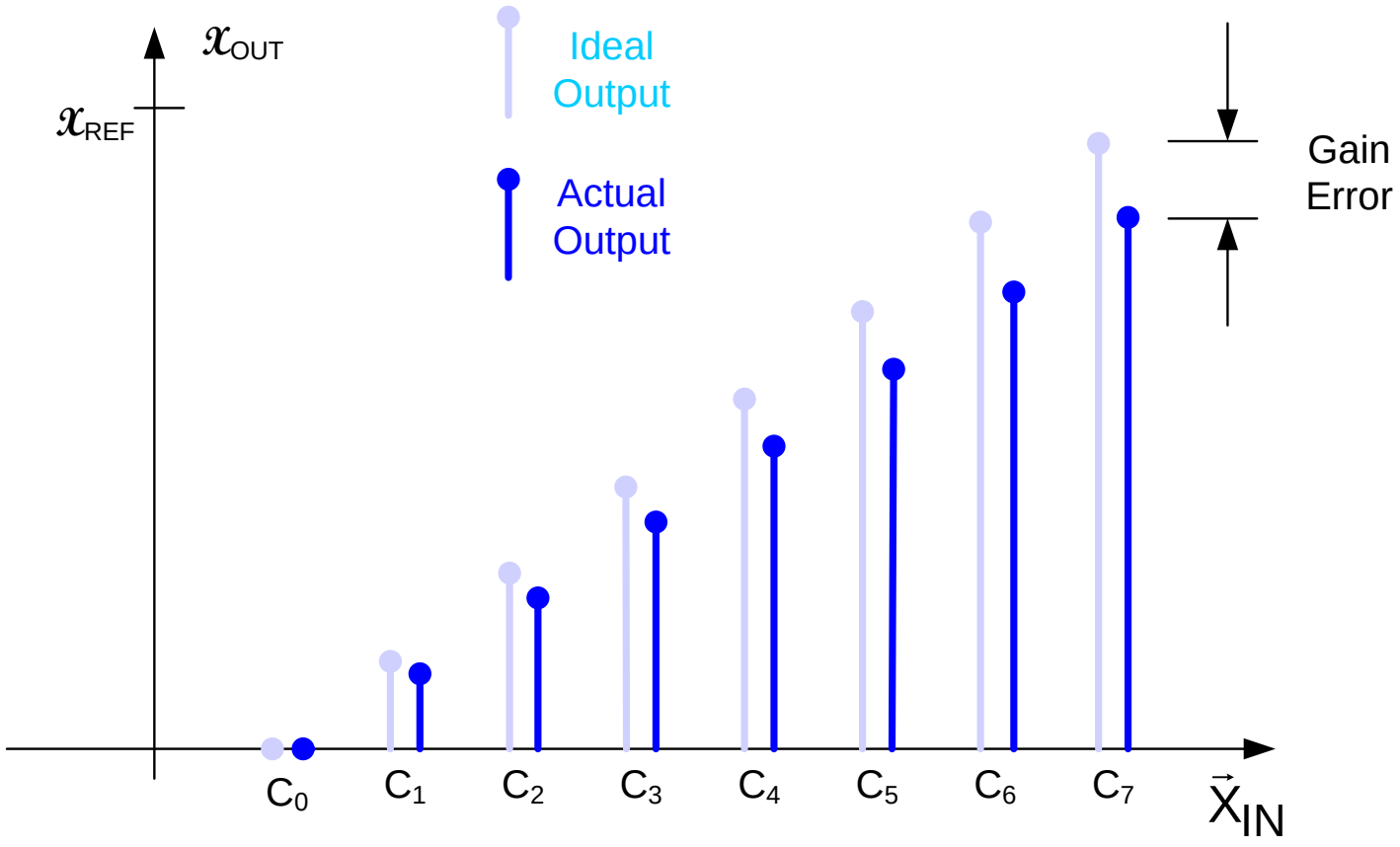


Offset relative to fit of data

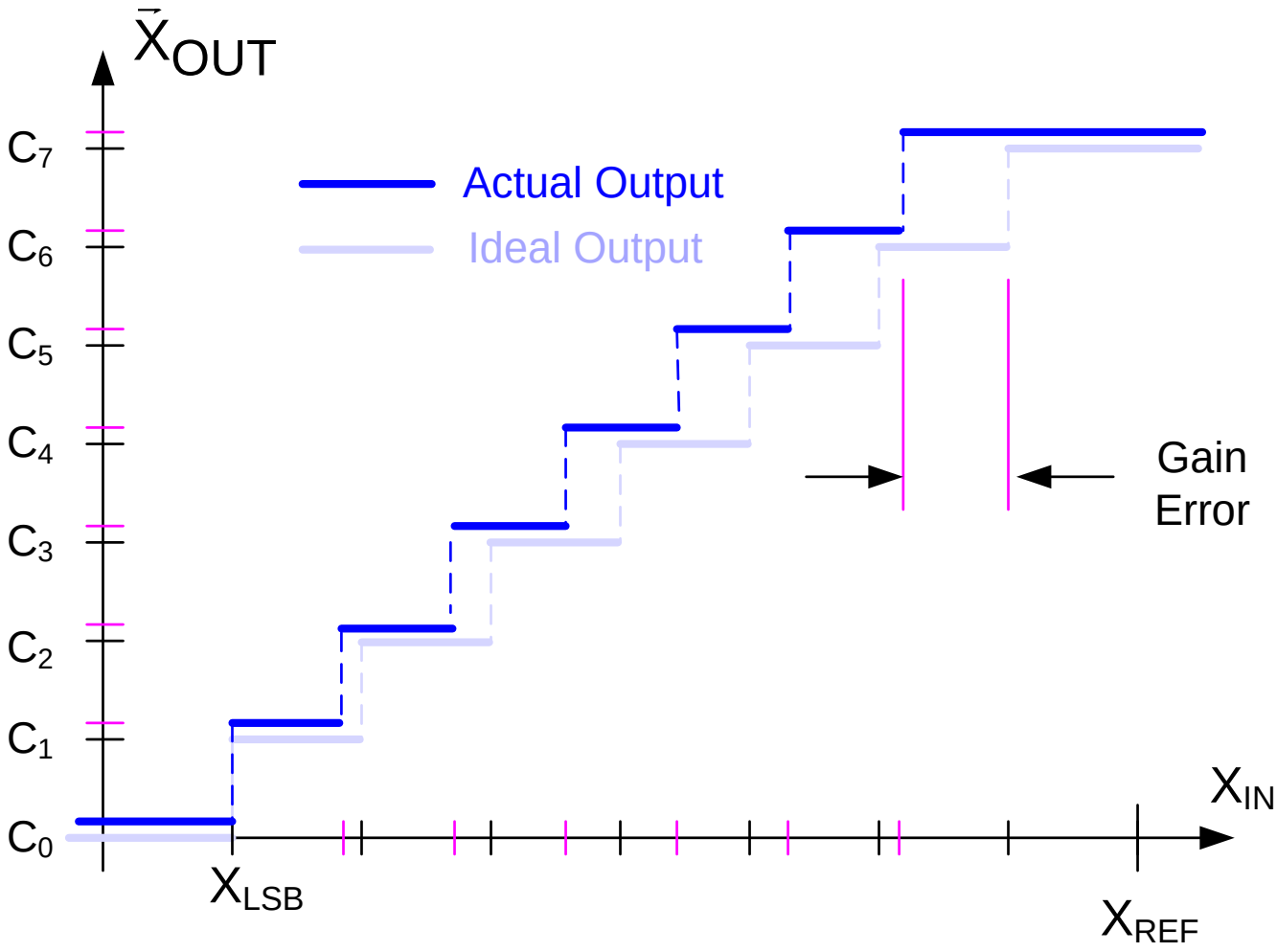
Gain and Gain Error

For DAC



Gain and Gain Error

For ADC



Gain and Offset Errors

- Fit line would give better indicator of error in gain but less practical to obtain in test
- Gain and Offset errors of little concern in many applications
- Performance of systems using data converters is often nearly independent of gain and offset errors
- Can be trimmed in field if gain or offset errors exist and are of concern

Performance Characterization of Data Converters

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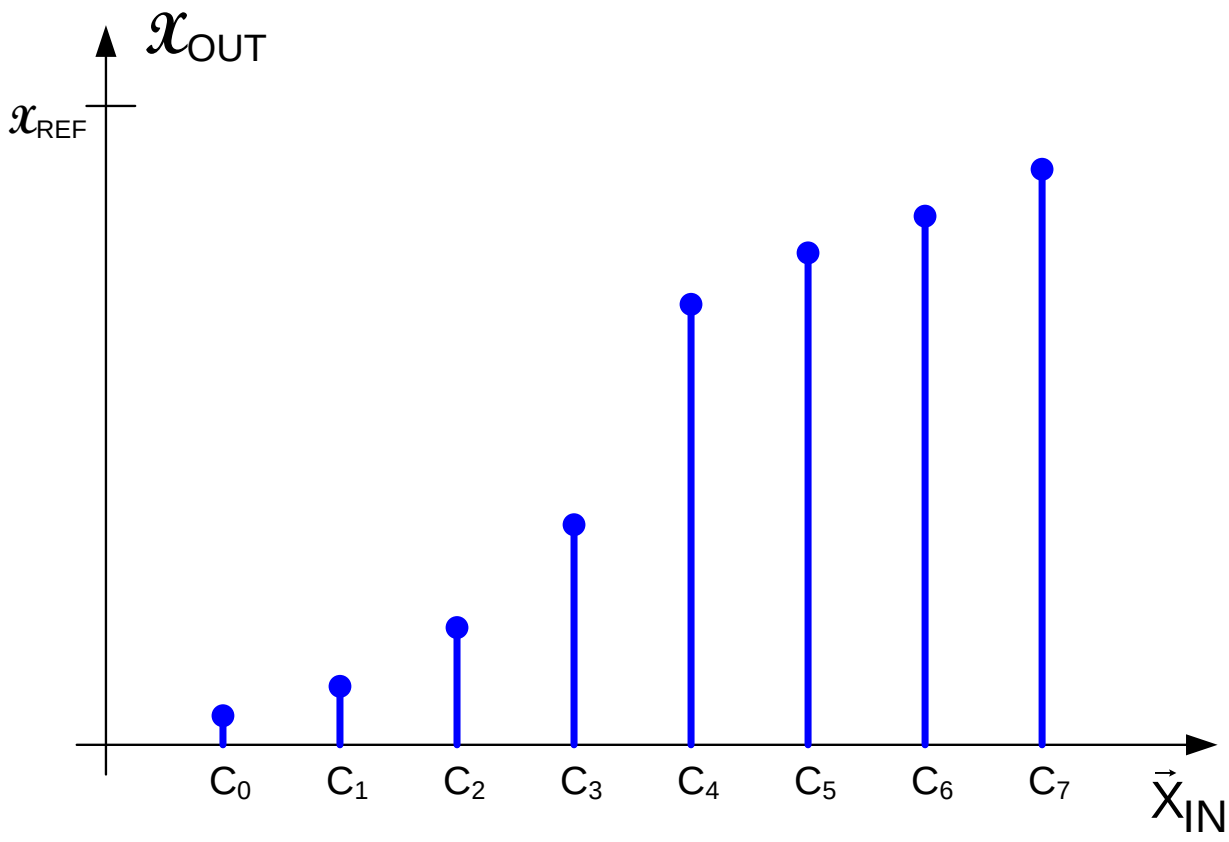
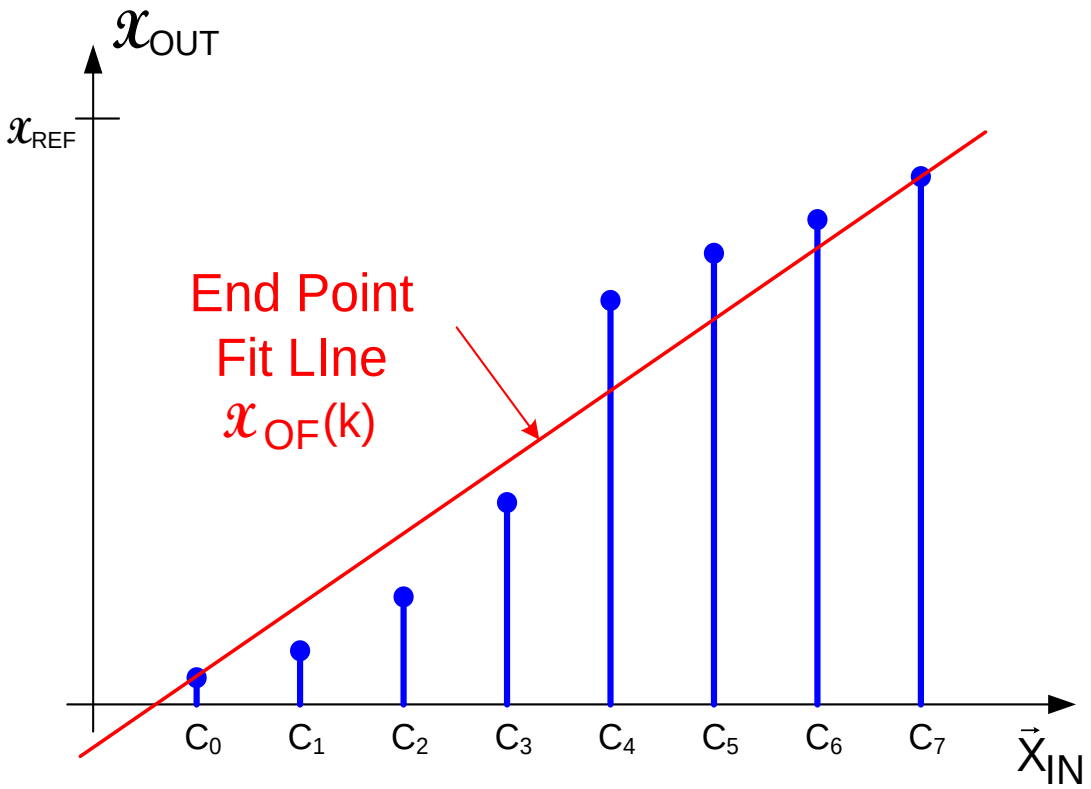
Integral Nonlinearity (DAC)

Nonideal DAC



Integral Nonlinearity (DAC)

Nonideal DAC

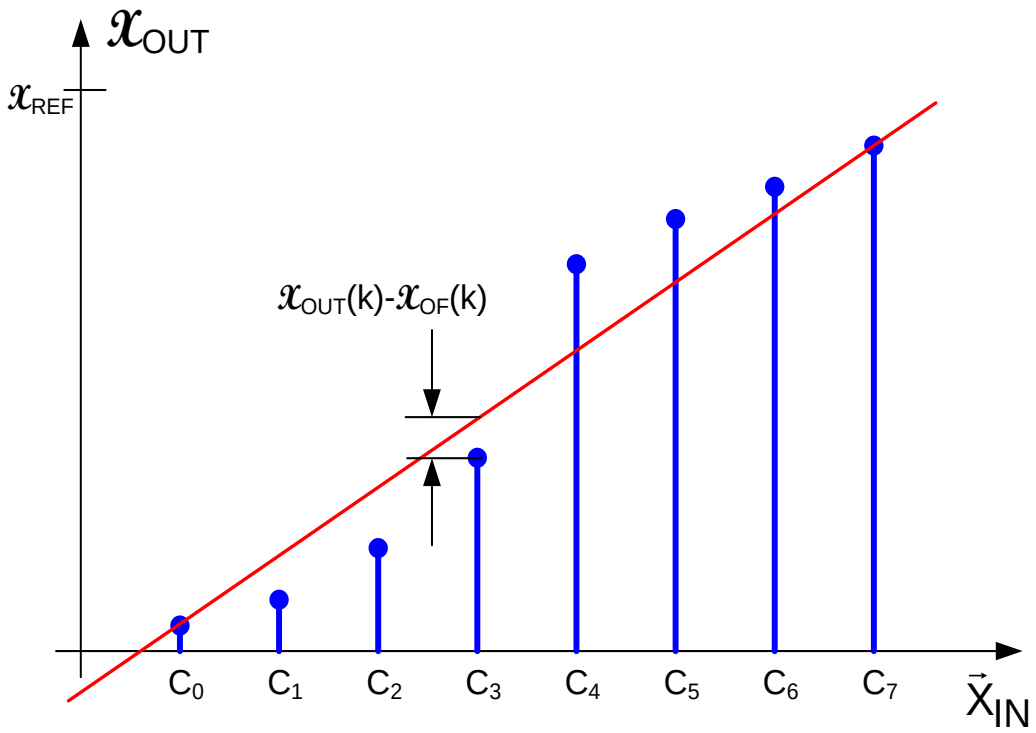


$$x_{OF}(k) = mk + x_{OUT}(0)$$

$$m = \frac{x_{OUT}(N\text{-}1) - x_{OUT}(0)}{N\text{-}1}$$

Integral Nonlinearity (DAC)

Nonideal DAC

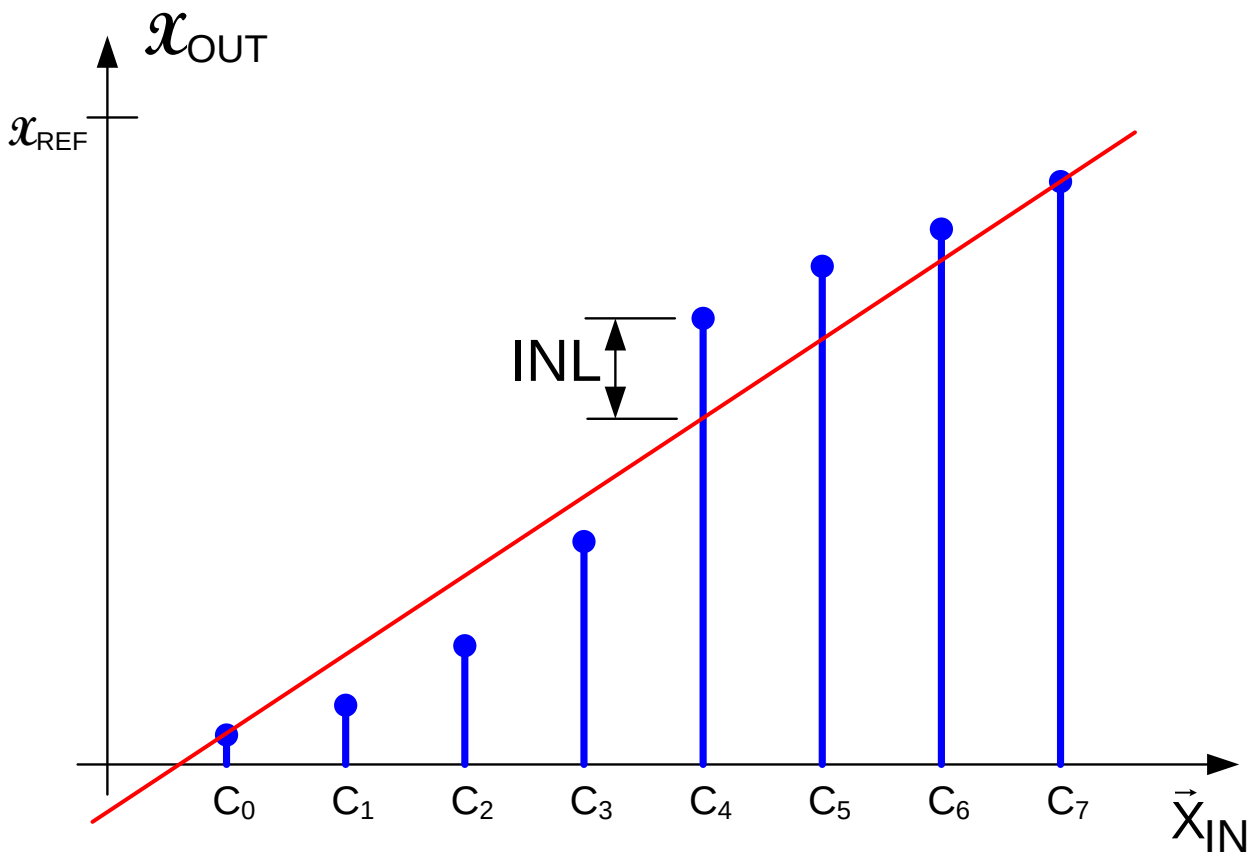


$$INL_k = x_{OUT}(k) - x_{OF}(k)$$

$$INL = \max_{0 \le k \le N-1} \{|INL_k|\}$$

Integral Nonlinearity (DAC)

Nonideal DAC



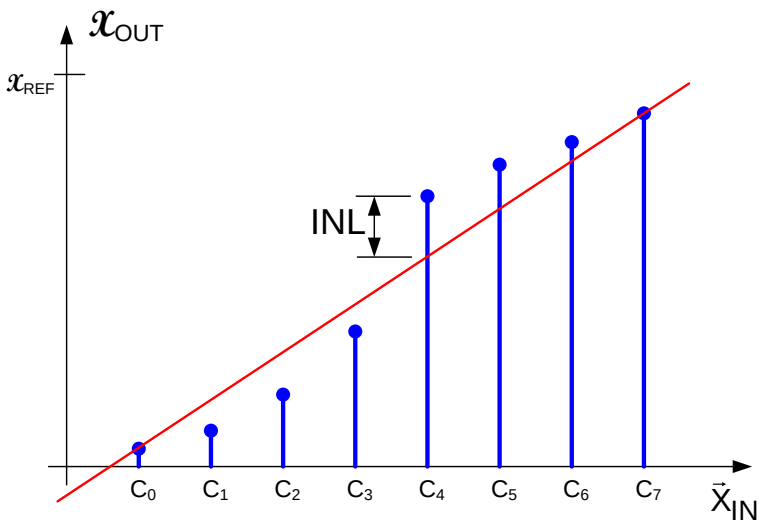
Integral Nonlinearity (DAC)

Nonideal DAC

INL often expressed in LSB

$$INL_k = \frac{x_{OUT}(k) - x_{OF}(k)}{x_{LSB}}$$

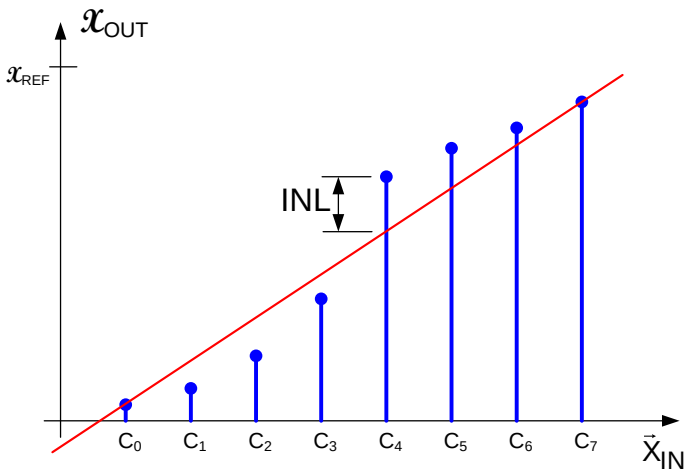
$$INL = \max_{0 \le k \le N-1} \left\{ |INL_k| \right\}$$



- INL is often the most important parameter of a DAC
- INL_0 and INL_{N-1} are 0 (by definition)
- There are N-2 elements in the set of INL_k that are of concern
- INL is almost always nominally 0 (i.e. designers try to make it 0)
- INL is a random variable at the design stage
- INL_k is a random variable for $0<k<N-1$
- INL_k and INL_{k+j} are almost always correlated for all k,j (not incl 0, N-1)
- Fit Line is a random variable
- INL is the N-2 order statistic of a set of N-2 correlated random variables
- Defining INL relative to a fit line would be more useful but more difficult to measure
- **INL is a parameter that is "attempting" to characterize the linearity of a DAC !**

Integral Nonlinearity (DAC)

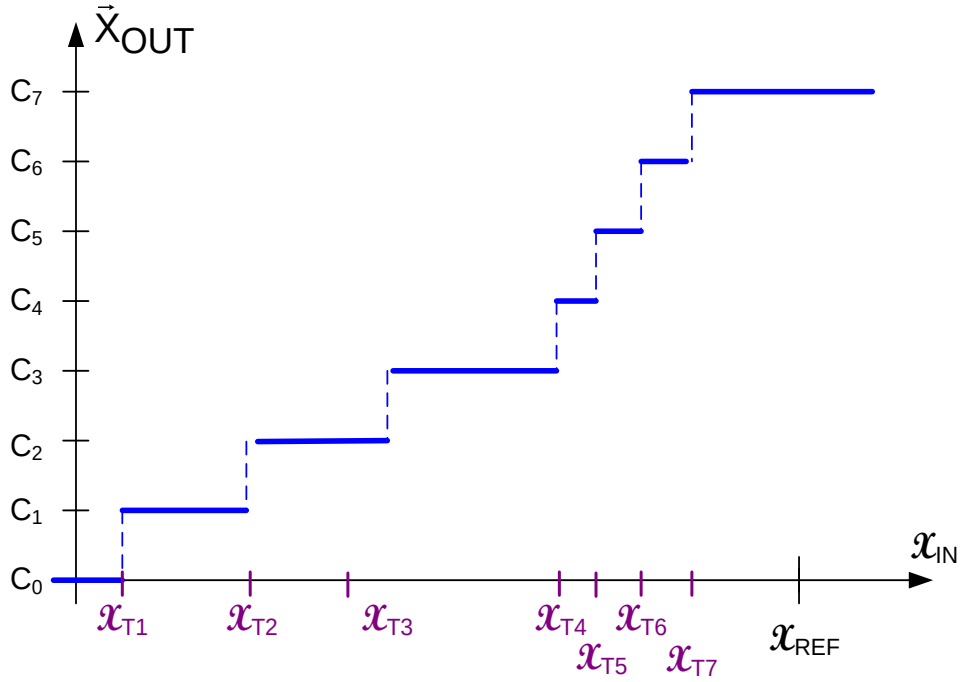
Nonideal DAC



- At design stage, INL characterized by standard deviation of the random variable
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - Model parameters become random variables
  - Process parameters affect multiple model parameters causing model parameter correlation
  - Simulation times can become very large
- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- Major effort in DAC design is in obtaining acceptable yield !
- Yield often strongly dependent upon matching of random variables!

Integral Nonlinearity (ADC)

Nonideal ADC



x_{Tk} is the transition input to code C_k

Transition points are not uniformly spaced !

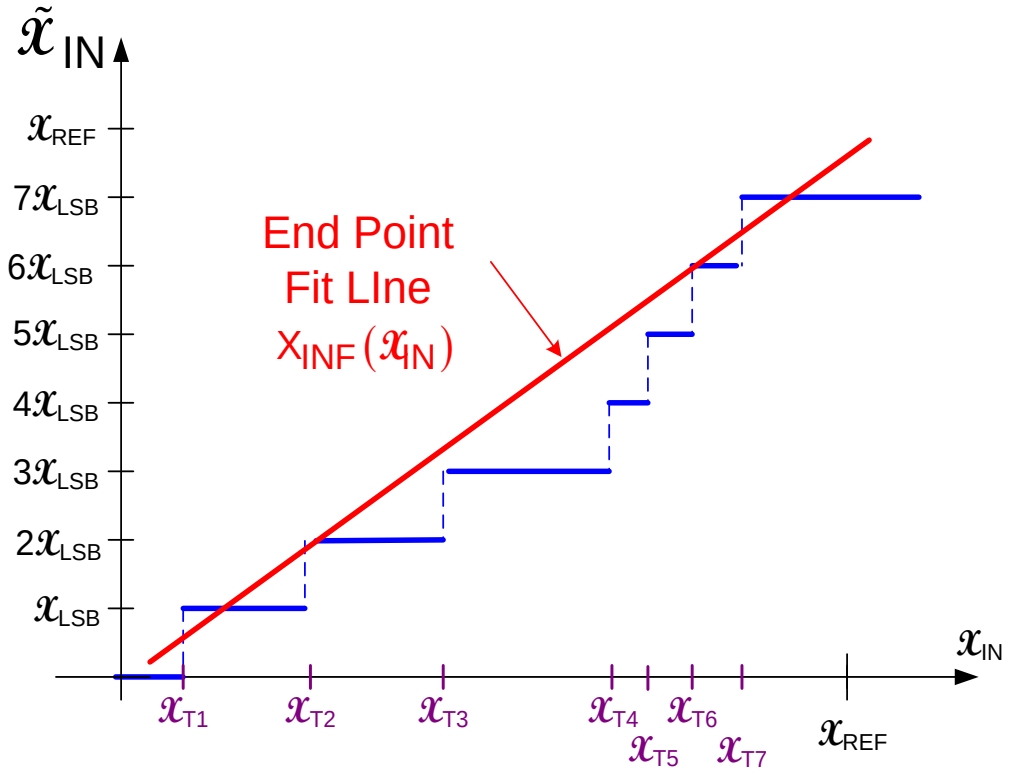
More than one definition for INL exists !

Will give two definitions here (second almost always used)

Note: is some cases the sequence $< x_{Tk} >$ may not be monotone

Integral Nonlinearity (ADC)

Nonideal ADC



Consider end-point fit line with interpreted output axis

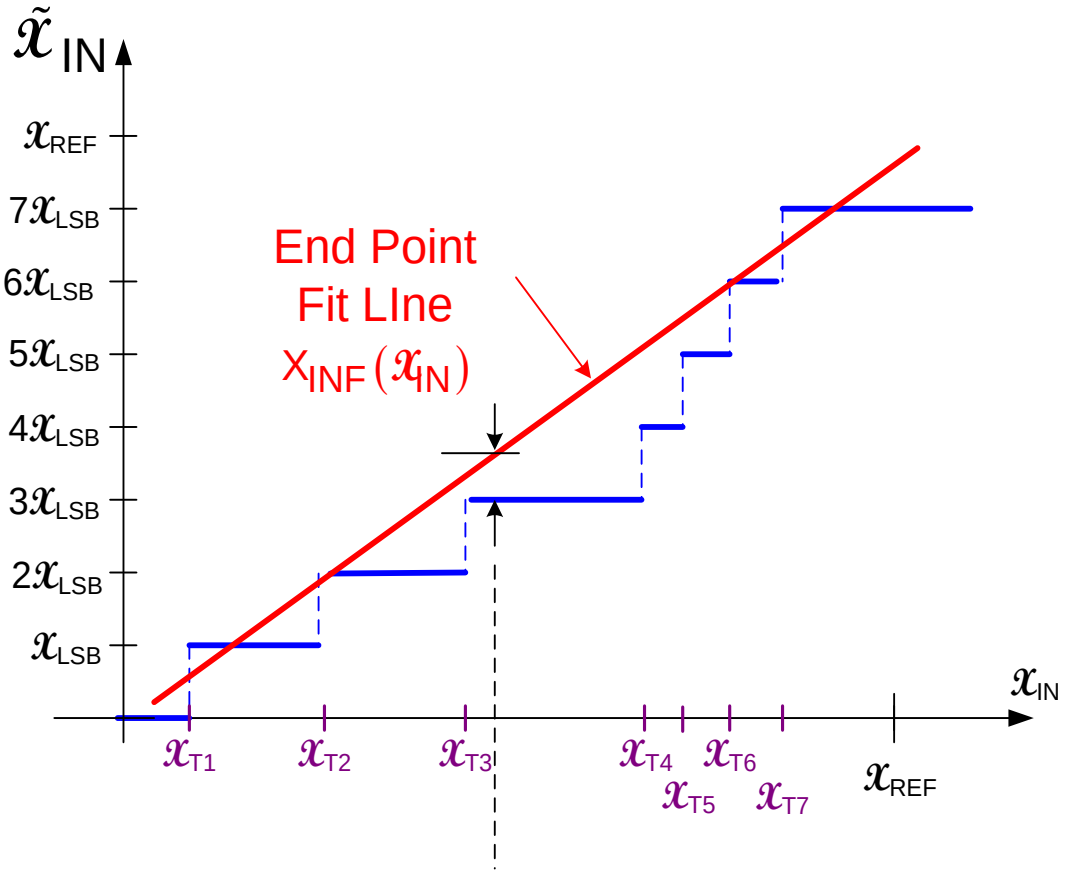
$$X_{INF}(x_{IN}) = m x_{IN} + \left(\frac{x_{LSB}}{2} - m x_{T1} \right)$$

$$m = \frac{(N-2)\, x_{LSB}}{x_{T7} - x_{T1}}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



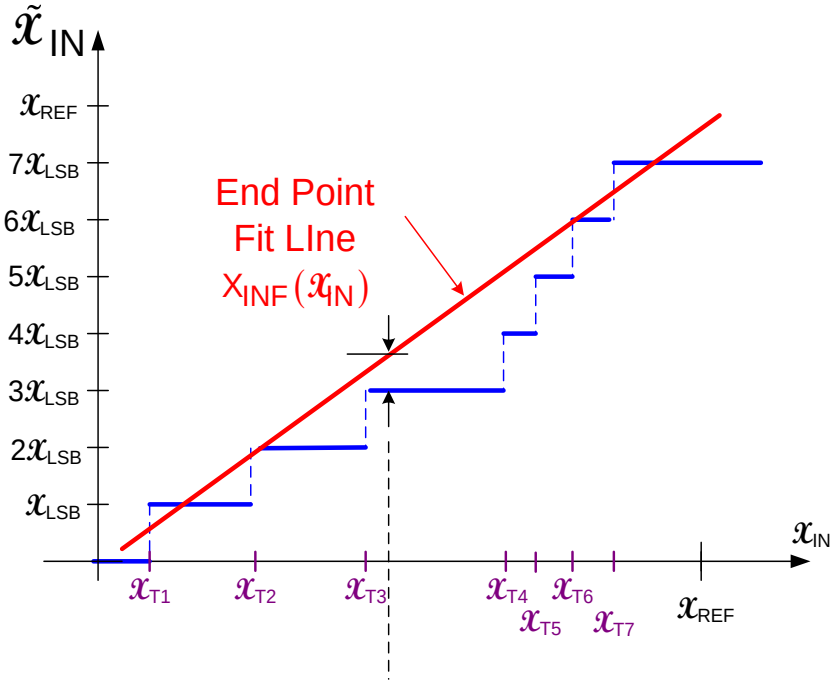
$$INL(x_{IN}) = \tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})$$

$$INL = \max_{0 \le x_{IN} \le x_{REF}} \left\{ \left| INL(x_{IN}) \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



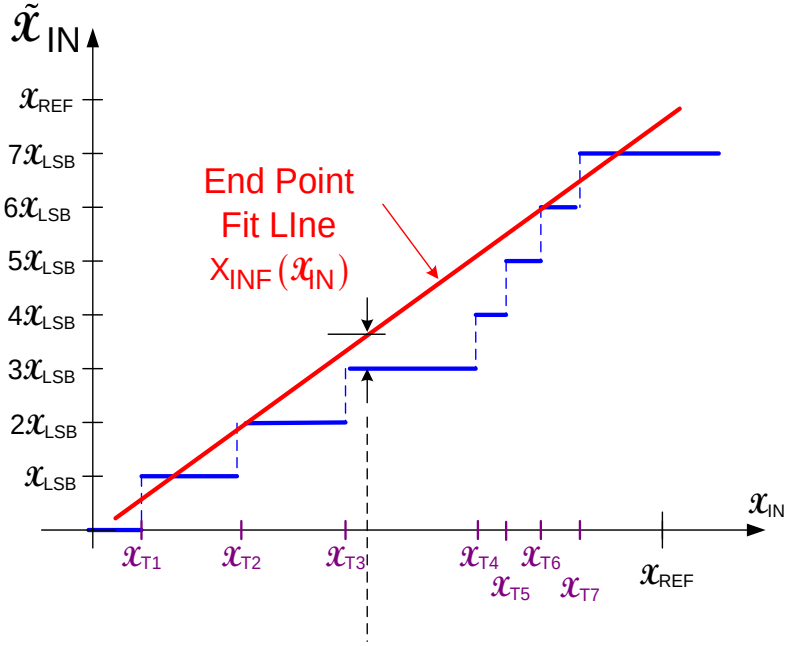
Often expressed in LSB

$$INL(x_{IN}) = \frac{\tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})}{x_{LSB}}$$

$$INL = \max_{0 \le x_{IN} \le x_{REF}} \left\{ \left| INL(x_{IN}) \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC



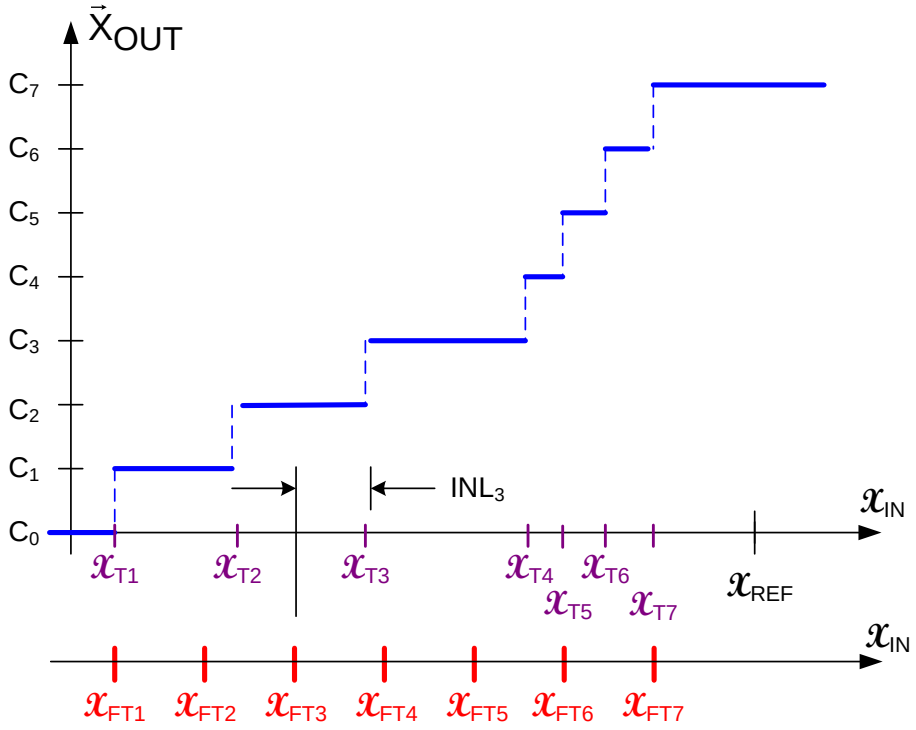
With this definition of INL, the INL of an ideal ADC is $x_{LSB}/2$ (for $x_{T1}=x_{LSB}$)

This is effective at characterizing the overall nonlinearity of the ADC but does not vanish when the ADC is ideal and the effects of the breakpoints is not explicit

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)



Place N-3 uniformly spaced points between X_{T1} and $X_{T(N-1)}$ designated x_{FTk}

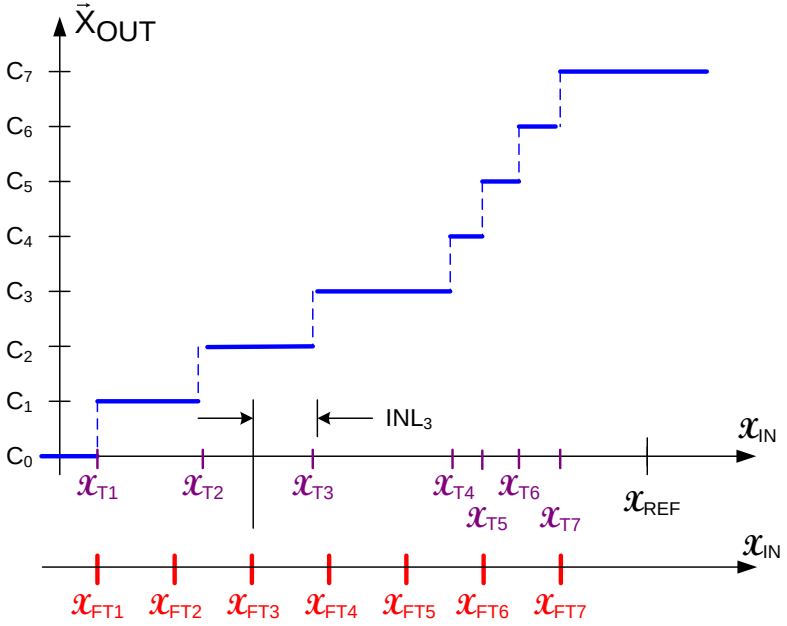
$$INL_k = x_{Tk} - x_{FTk} \qquad 1 \le k \le N\text{-}2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)



Often expressed in LSB

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$

For an ideal ADC, INL is ideally 0

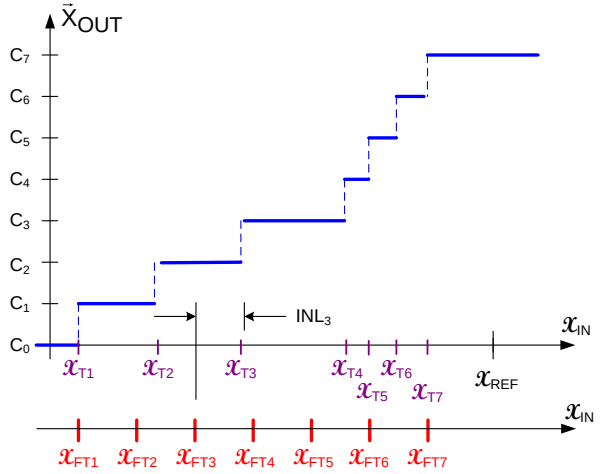
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



- INL is often the most important parameter of an ADC
- INL_1 and INL_{N-1} are 0 (by definition)
- There are N-3 elements in the set of INL_k that are of concern
- INL is a random variable at the design stage
- INL_k is a random variable for 0<k<N-1
- INL_k and INL_{k+j} are correlated for all k,j (not incl 0, N-1) for most architectures
- Fit Line (for cont INL) and uniformly spaced break pts (breakpoint INL) are random variables
- INL is the N-3 order statistic of a set of N-3 correlated random variables (breakpoint INL)
- Defining INL relative to a fit line would be more useful but more difficult to measure
- **INL is a parameter that is "attempting" to characterize the linearity of an ADC !**

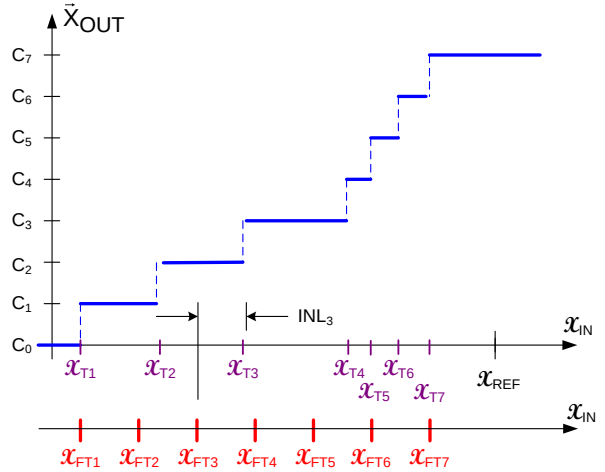
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)

$$INL_k = \frac{x_{Tk} - x_{FTl}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



What if there are less than N-3 internal transitions?

- Assume N-k internal transitions where k>3
- Data converter may still perform quite well !
- Insert N-k uniformly spaced values and use previous definition
- Unusual issues can crop up when testing data converters and it is important to have well-defined algorithms for handling these situations

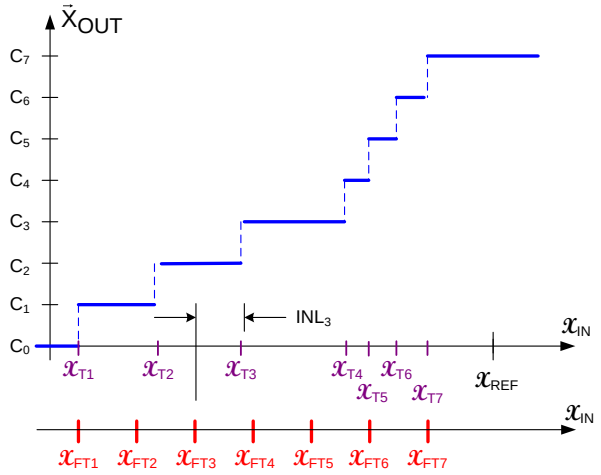
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



- At design stage, INL characterized by standard deviation of many random variables
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - -Model parameters become random variables
  - -Process parameters affect multiple model parameters causing model parameter correlation
  - -Simulation times can become very large

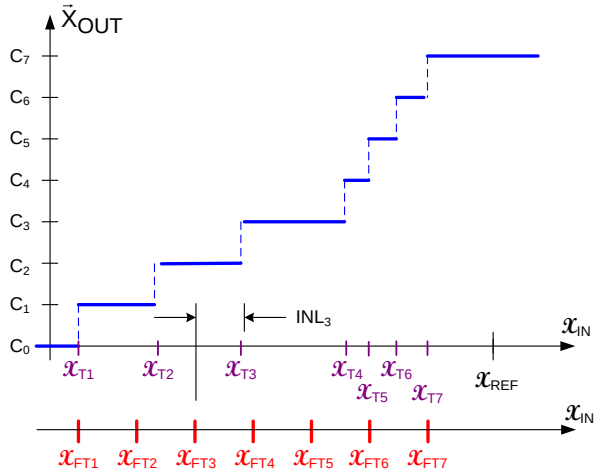
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- INL of $\frac{x_{LSB}}{2}$ often considered acceptable (this is the ideal value of the continuous-input INL)

- Major effort in ADC design is in obtaining an INL acceptable yield !
- Yield often strongly dependent upon matching of random variables !

Characteristics Dominantly Depend Upon Random Variables

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Characteristics Dominantly Depend Upon Random Variables

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Methods of Characterizing how Random Variables Affect Performance

- Analytical Statistical Formulation and Analysis
- MATLAB Simulations (often using Monte-Carlo Analysis)
- Spectre/Spice Monte-Carlo Simulations
- Ignore Effects of Random Effects

How important is statistical characterization of data converters?

How important is statistical analysis?

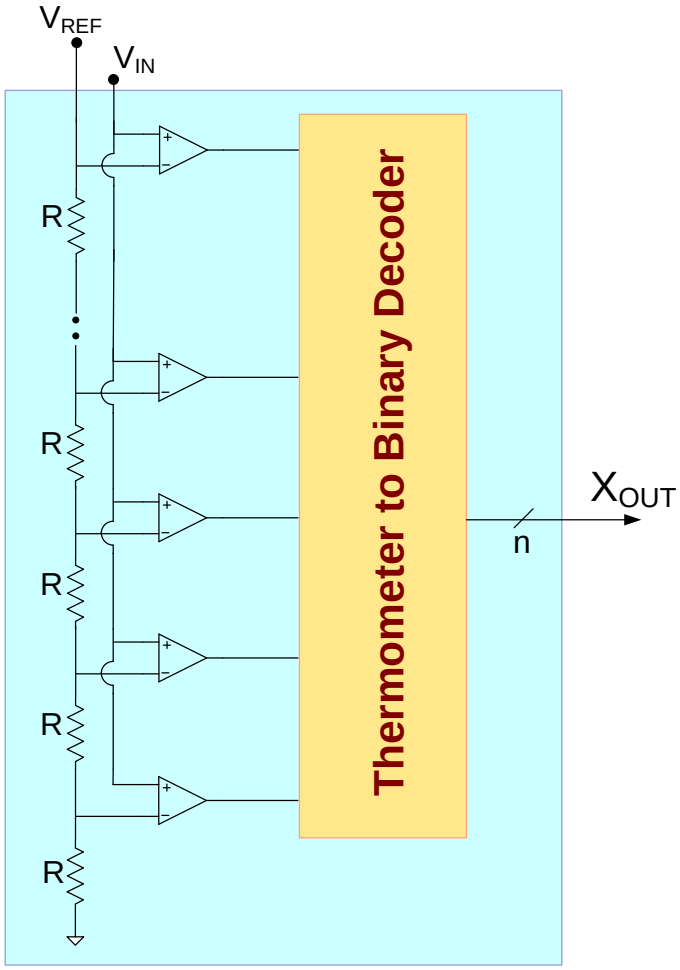
Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB

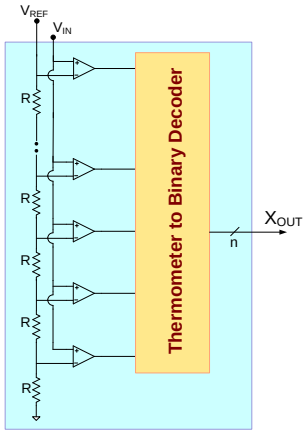
Why this assumption?

Case 1

Determine the yield if V_{OS} has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV



How important is statistical analysis?



Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB

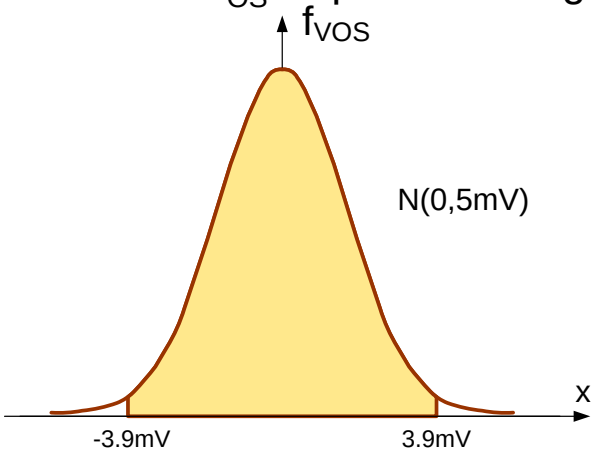
Case 1

Determine the yield if V_{OS} has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV

½ LSB = $1V/(2^{(7+1)})$=3.9mV

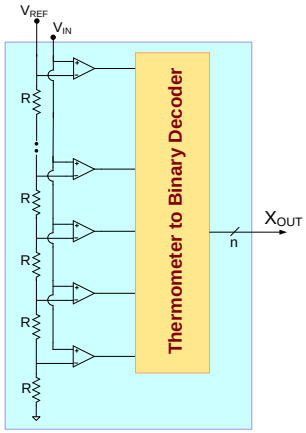
The probability that a single comparator meets the V_{OS} requirement is given by

$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS} dV$$



How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 1 σ_{VOS}=5mV

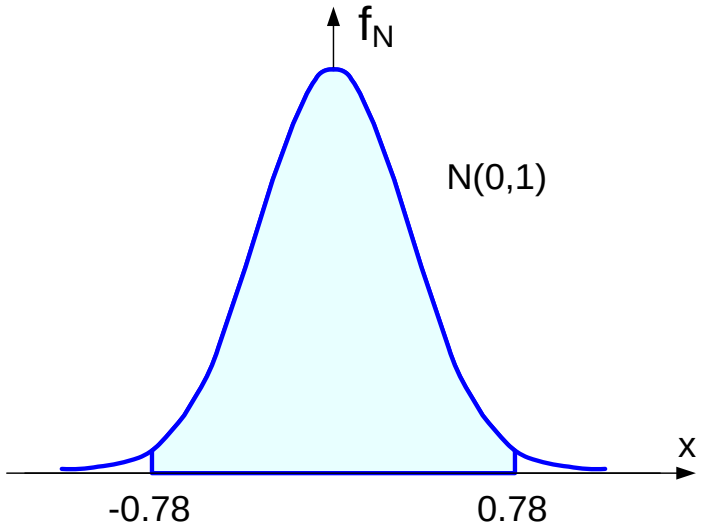
$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS} dV$$

Define $X_N = V_{OS}/\sigma$

$$P_{COMP} = \int_{-X_N}^{X_N} f_N dx$$

X_N=3.9mV/5mV=0.78

$$P_{COMP} = \int_{-0.78}^{0.78} f_N dx$$

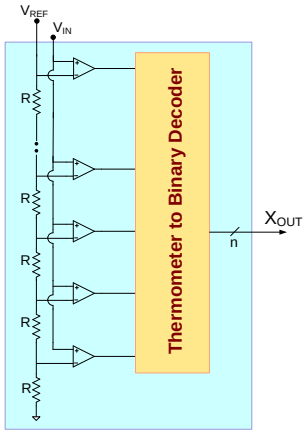


$$P_{COMP} = 2 \bullet F_N(0.78) - 1 = 2 \bullet .7823 - 1 = 0.565$$

Each comparator has 56.5% yield

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 1 σ_{VOS}=5mV

P_{COMP} = 0.565

Since all comparators must be good, the ADC yield is

$$Y_{ADC}=(P_{COMP})^{127}=(0.565)^{127}$$

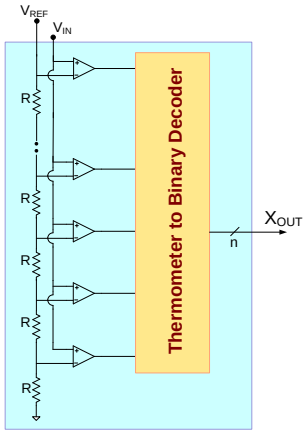
$$Y_{ADC}=3.2\bullet10^{-32}$$

This yield is essentially 0 and a standard deviation of 5mV is even not trivial to obtain with MOS comparators !

The effects of statistical variation can have dramatic effects on yield of data converters !

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 1 σ_{VOS}=5mV

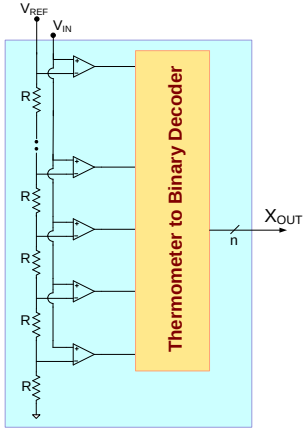
Since all comparators must be good, the ADC yield is

$$Y_{ADC}=3.2\bullet10^{-32}$$

Note: The specification in this example that requires no comparator has an offset voltage of larger than 0.5LSB may not be a good performance specification as the FLASH ADC may actually perform reasonably well even if some comparators have an offset that is larger than 0.5LSB. A more useful requirement might be that there be no bubbles in the thermometer code output. Certainly if all comparators have an offset that is at most 0.5LSB, there will be no bubbles in the output code attributable to comparator offset but a modestly weaker constraint can also guarantee there are no bubbles. With the 0.5LSB assumption, a specification that was dependent upon 127 uncorrelated random variables was obtained which made the analysis quite easy. A “no bubble” specification could be approximated by stating that the maximum of the 127 V_{OSk}-V_{OSk-1}must be less than V_{LSB}. This becomes an order statistic of 127 Gaussian random variables which is analytically intractable.

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 2 Repeat the previous example if σ_{VOS}=1mV

$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS}\,dV \quad \rightarrow \quad X_N = 3.9mV/1mV = 3.9$$

$$P_{COMP} = \int_{-3.9}^{3.9} f_N\,dx \qquad P_{COMP} = 2 \bullet F_N(3.9) - 1 = 2 \bullet 0.999952 - 1 = 0.999904$$

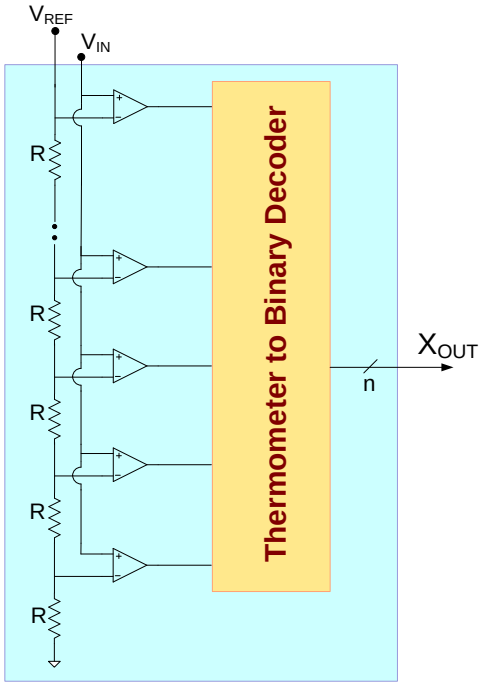
$$Y_{ADC} = (P_{COMP})^{127} = (0.999904)^{127}$$

$$Y_{ADC} = 0.988$$

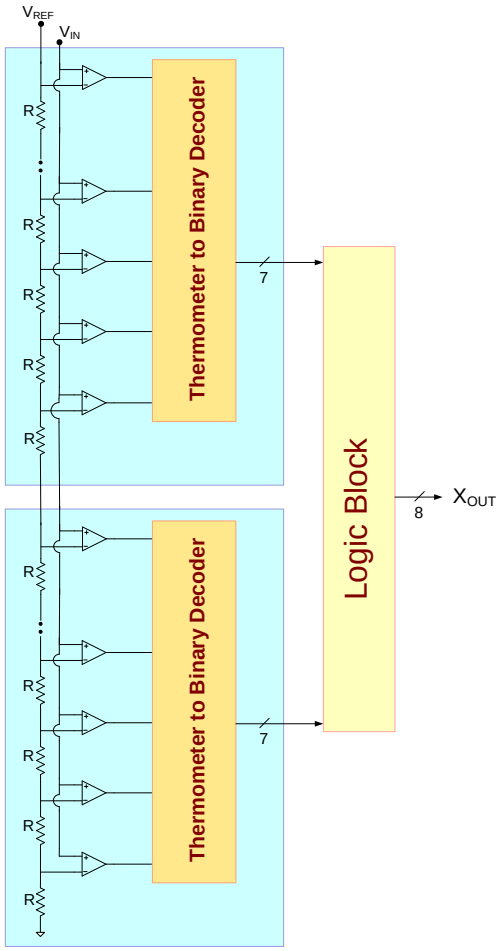
This modest change in the offset voltage has increased the yield to 98.8%

How important is statistical analysis?

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



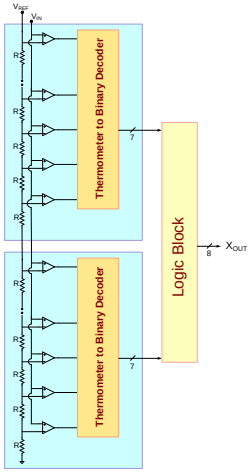
Y_{ADC}=98.8%



Y_{ADC}=?

How important is statistical analysis?

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



Since one additional bit has been added, V_{LSB} will decrease From 7.8mV to 3.9mV. Thus ½ LSB will be reduced to 1.95mV

$$P_{COMP} = \int_{-1.95mV}^{1.95mV} f_{VOS}\,dV$$

With the same σ_{VOS}=1mV, X_N=1.95mV/1mV=1.95

$$P_{COMP} = \int_{-1.95}^{1.95} f_N\,dx \qquad P_{COMP} = 2 \bullet F_N(1.95) - 1 = 2 \bullet 0.97441 - 1 = 0.9488$$

$$Y_{ADC} = (P_{COMP})^{255} = (0.9488)^{255}$$

$$Y_{ADC} = 1.52 \bullet 10^{-6}$$

This seemingly simple extension of a circuit with a very high yield has essentially no yield !

How important is statistical analysis?

- Statistical analysis of data converters is critical
- Some architectures are more sensitive than others to statistical variations in components
- The onset of yield loss due to statistical limitations is generally quite abrupt
- and can have disastrous effects if not considered as part of the design process

Recall examples where σ_{VOS}=5mV compared with σ_{VOS}=1mV

- Substantially over-designing to avoid concerns about statistical yield loss is not a practical solution since the area penalty, the speed penalty, and the power penalty are generally quite severe

For the effects of local random variations of a parameter X, generally

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

where A_C is the area of the matching critical components and A_0 is a process parameter

Importance of statistical analysis – example

What changes in area would be needed to decrease σ_{VOS} from 5mV to 1mV?

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

$$\left.\begin{aligned} \sigma_{X_5} &= \theta \frac{A_0}{\sqrt{A_{C_5}}} \\ \sigma_{X_1} &= \theta \frac{A_0}{\sqrt{A_{C_1}}} \end{aligned}\right\} \quad \Rightarrow \quad \frac{\sigma_{X_5}}{\sigma_{X_1}} = \frac{\sqrt{A_{C_1}}}{\sqrt{A_{C_5}}} = 5$$

$$A_{C_1} = 25 A_{C_5}$$

Equivalent Number of Bits (ENOB)

- Often the performance of an n-bit data converter is not commensurate with that of an ideal n-bit data converter but more like that of an n-k bit data converter
- The equivalent number of bits (ENOB) is often used to characterize the actual level of performance
- Different ENOB definitions depending upon which characterization parameter is of interest

  (e.g. INL, SFDR, SNR, …)

INL-based ENOB

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is $X_{LSB}/2$

Assume $$INL = \upsilon X_{LSBR} = \upsilon \frac{X_{REF}}{2^{n_R}}$$

where X_{LSBR} is the LSB based upon the defined resolution , n_R

Define the equivalent LSB by $$X_{LSBE} = \frac{X_{REF}}{2^{n_{EQ}}}$$

Thus (substituting for X_{REF} into INL expression):

$$INL = \upsilon \frac{2^{n_{EQ}}}{2^{n_R}} X_{LSBE} = \left[\upsilon 2^{n_{EQ}+1-n_R} \right] \frac{X_{LSBE}}{2}$$

Since an ideal ADC has an INL of $X_{LSB}/2$, Setting term in [ ] to 1, can solve for n_{EQ} to obtain

$$ENOB = n_{EQ} = \log_2\left(\frac{1}{2\theta}\right) = n_R - 1 - \log_2(\upsilon)$$

where n_R is the defined resolution

INL-based ENOB

$$ENOB = n_R - 1 - \log_2(\upsilon)$$

Consider an ADC with specified resolution of n_R and INL of v LSB

υ	ENOB
½	n_R
1	n_R-1
2	n_R-2
4	n_R-3
8	n_R-4
16	n_R-5

Though based upon the continuous-INL definition, often used to define ENOB from INL viewpoint

ANALOG DEVICES

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet

$120 in 1000's

AD9467

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - ~~DNL = ±0.5 LSB typical~~
  - INL = ±3.5 LSB typical
- ~~2 V p-p to 2.5 V p-p (default)~~ differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM

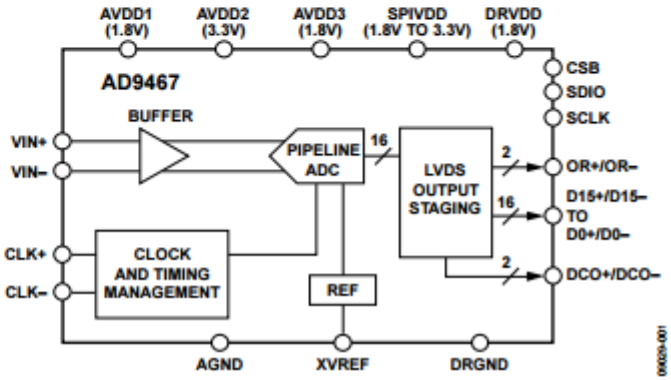


Figure 1.

ENOB $= n_R\text{-}1\text{-}\log_2(\upsilon) = 16 - 1 - 1.85 \cong 13.15$

Is this close to 16-bit performance?

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

Test Setup Quite Sophisticated

From ADI AN-835

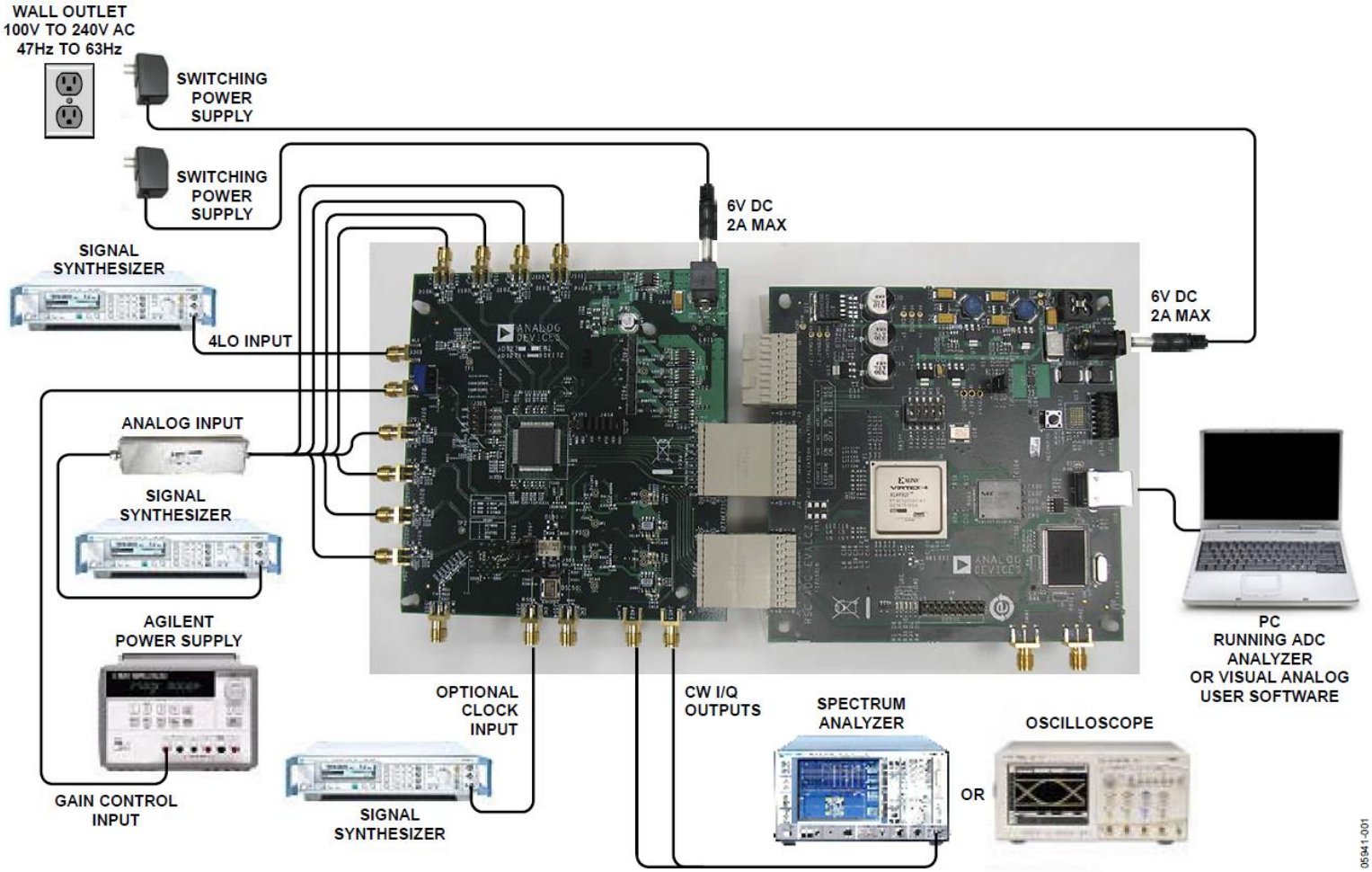


Figure 1. Typical Characterization Test Setup

Test Setup Quite Sophisticated

From ADI AN-835

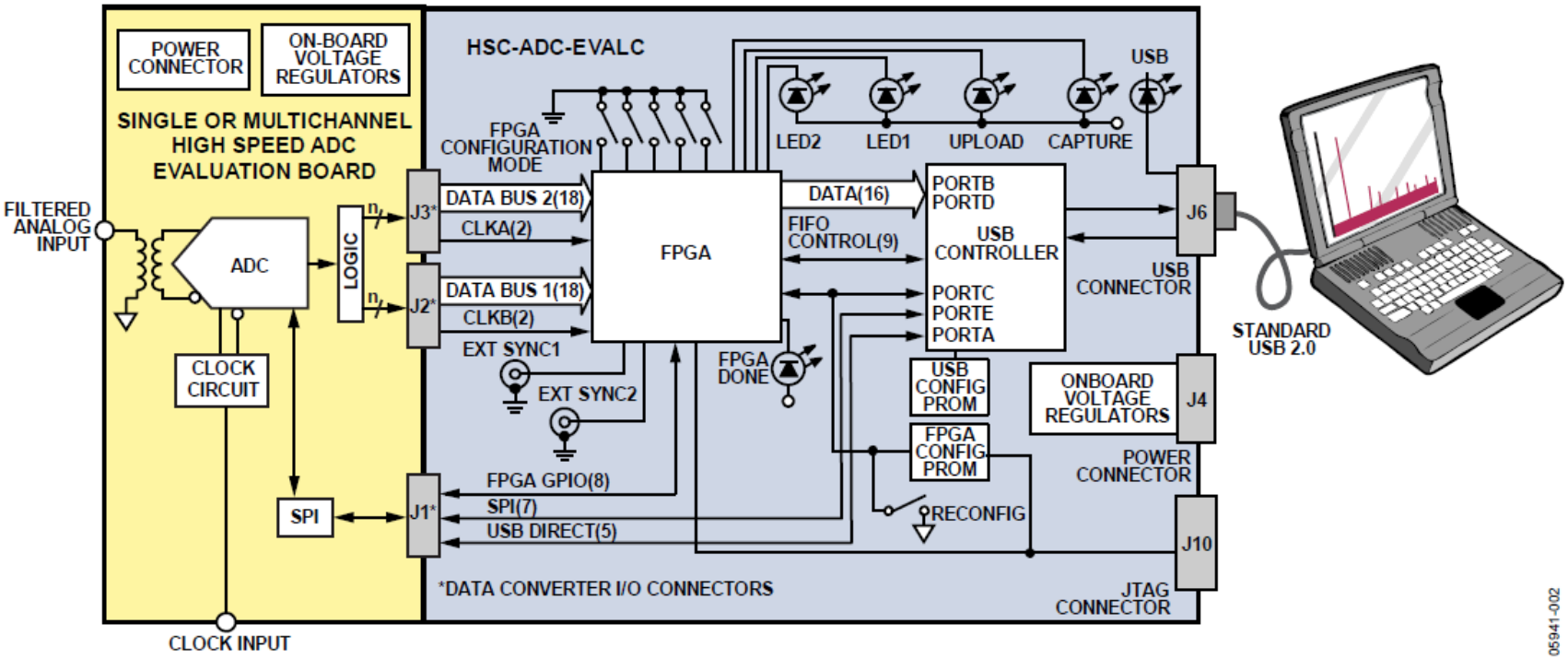


Figure 2. Typical HSC-ADC-EVALC Evaluation Platform

Test Setup Quite Sophisticated

From ADI AN-835

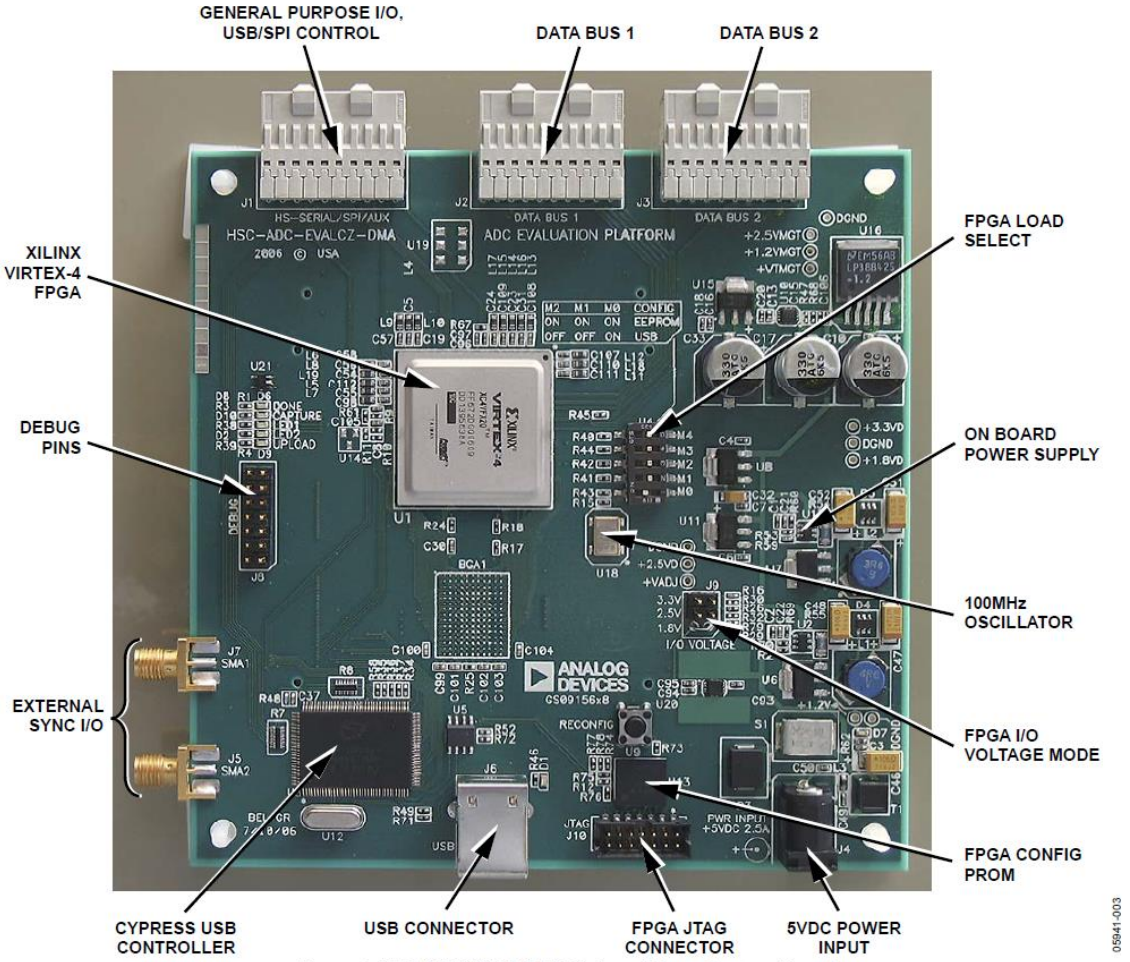


Figure 3. HSC-ADC-EVALC: FPGA-Based Data Capture Board

Can we depend on this “13-bit” INL performance?

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

$$\text{ENOB} = n_R\text{-}1\text{-}\log_2(\upsilon) = 16 - 1 - 3.58 \cong 11.42$$

From INL viewpoint, performance is about 4.5 bits less than physical resolution but does have other attractive properties

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

- Can be defined different ways
- Only given as typical

Stay Safe and Stay Healthy !

End of Lecture 2